Schematics Page Index (Title / Revision / Change Date)

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19	ICH8-M(LPC,IDE,SATA)2/5			54	AUDIO(EQ)				
20	ICH8-M(GPIO) 3/5			55	AEC(FM2010)				
21	ICH8-M(POWER) 4/5			56	Power Design Diagram				
22	ICH8-M(GND) 5/5			57	DCIN				
23	SATA HDD/CD-ROM			58	SYSPWR(+3VALW/+5VALW)				
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25	EC (KB3910S)			60	VHCORE(ISL6262A)				
26	Flash ROM XBUS/SPI			61	VGA POWER(GMCH)				
27	Mini Card			62	SYSPWR(+1_5VRUN/+1_05VRUN)				
28	FAN/HWM/HW THERMAL PROTECT			63	HDD PWR (+12VRUN)				
29	EXPRESS Card/CAM/RF KB			64	Others power plan				
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35	LAN (1/2)								

BOM OPTION

COMPONENT	WINBOND	ENE
C72,RP9	NC	STUFF
R110	4.7K	47K

COMPONENT	Samsung	Qimonda
R26	Stuff	NC
R39	NC	Stuff

PCB P/N:	__-_____-__SA
	__-_____-__SA
	__-_____-__SA

Project Code & Schematics Subject: M630/M640 Main Board

	M630GM	M630PM	M640GM	M640PM
CR_	V		V	
NV_		V		V
NC_	V	V	V	V
Exclude "M640_"	V	V		
(Default)			V	

P. Leader	Check by	Design by

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Title: *Index Page*

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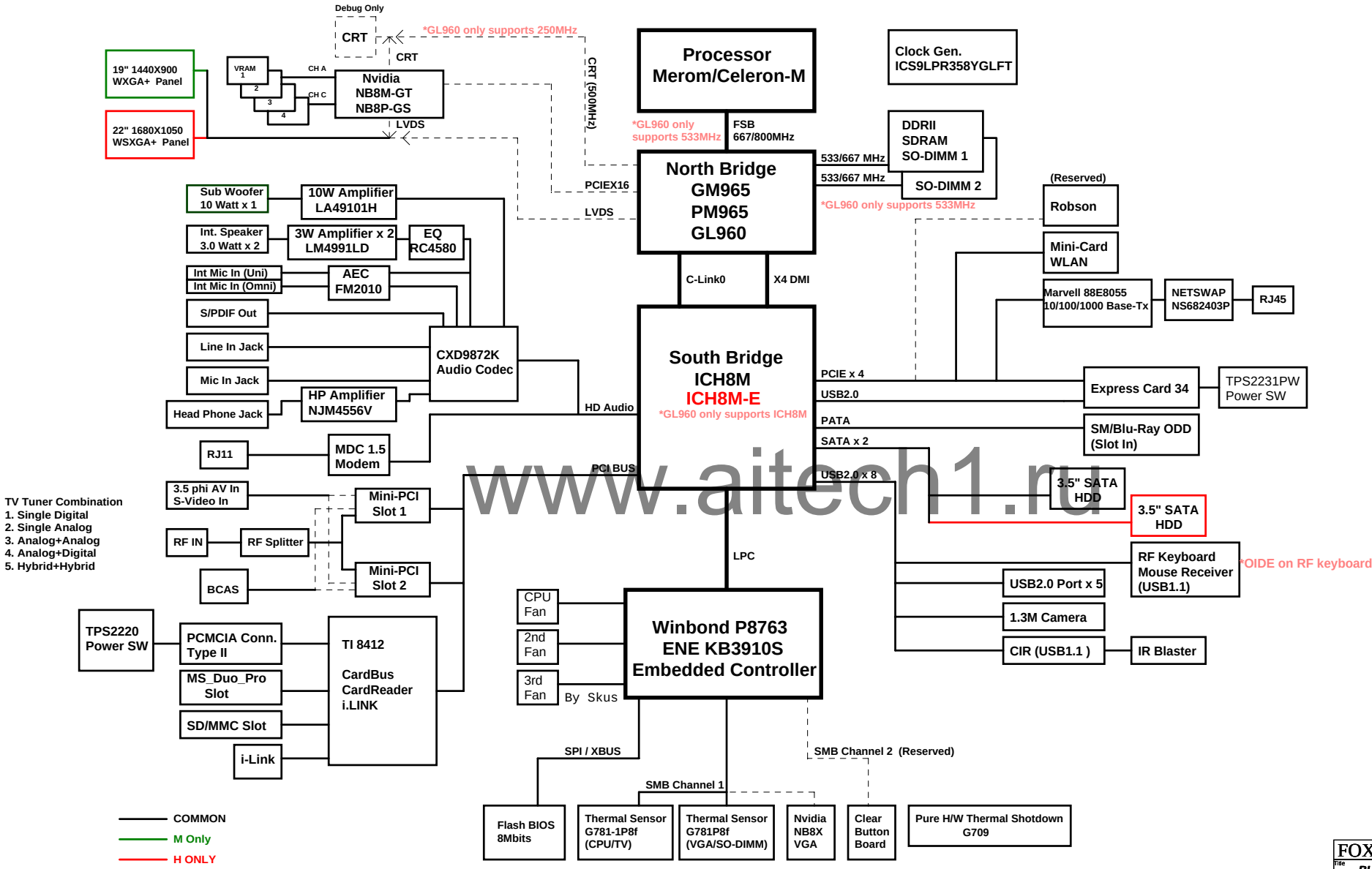
M630/640 Block Diagram (19"/22" Wide Screen)



SYSTEM DC/DC MAX8734A P.57

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC SC339 P.61

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_5VRUN

SC486 P.58

INPUTS	OUTPUTS
DCBATOUT	+1_8V_S3_SUS +0_9V_S3_SUS

CPU DC/DC ISL6262A P.59

INPUTS	OUTPUTS
DCBATOUT	VHCORE

CPU DC/DC MAX8546 P.62

INPUTS	OUTPUTS
DCBATOUT	+12VRUN

SYSTEM DC/DC GMT923/GMT966 P.63

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_25VRUN

SYSTEM DC/DC 0Z811 GMT966(PEX_VDD) P.60

INPUTS	OUTPUTS
DCBATOUT DCBATOUT +1_8V_S3_SUS	+1_05VRUN NV_VDD PEX_VDD

Nvidia Gfx VDDC

INPUTS	OUTPUTS
+VGFX_CORE	+1_05VRUN (or NV_VDD)

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Title: BLOCK DIAGRAM

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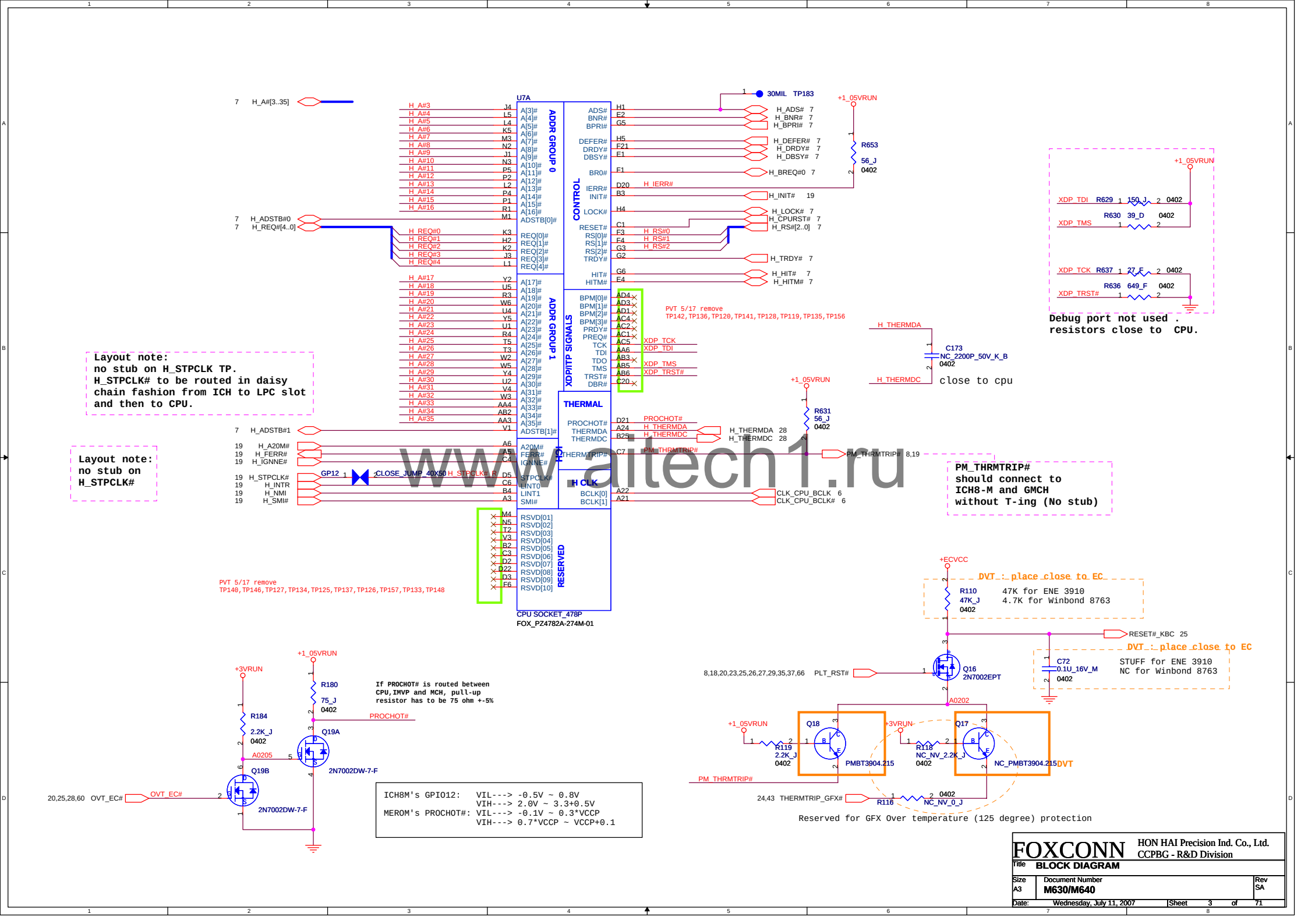

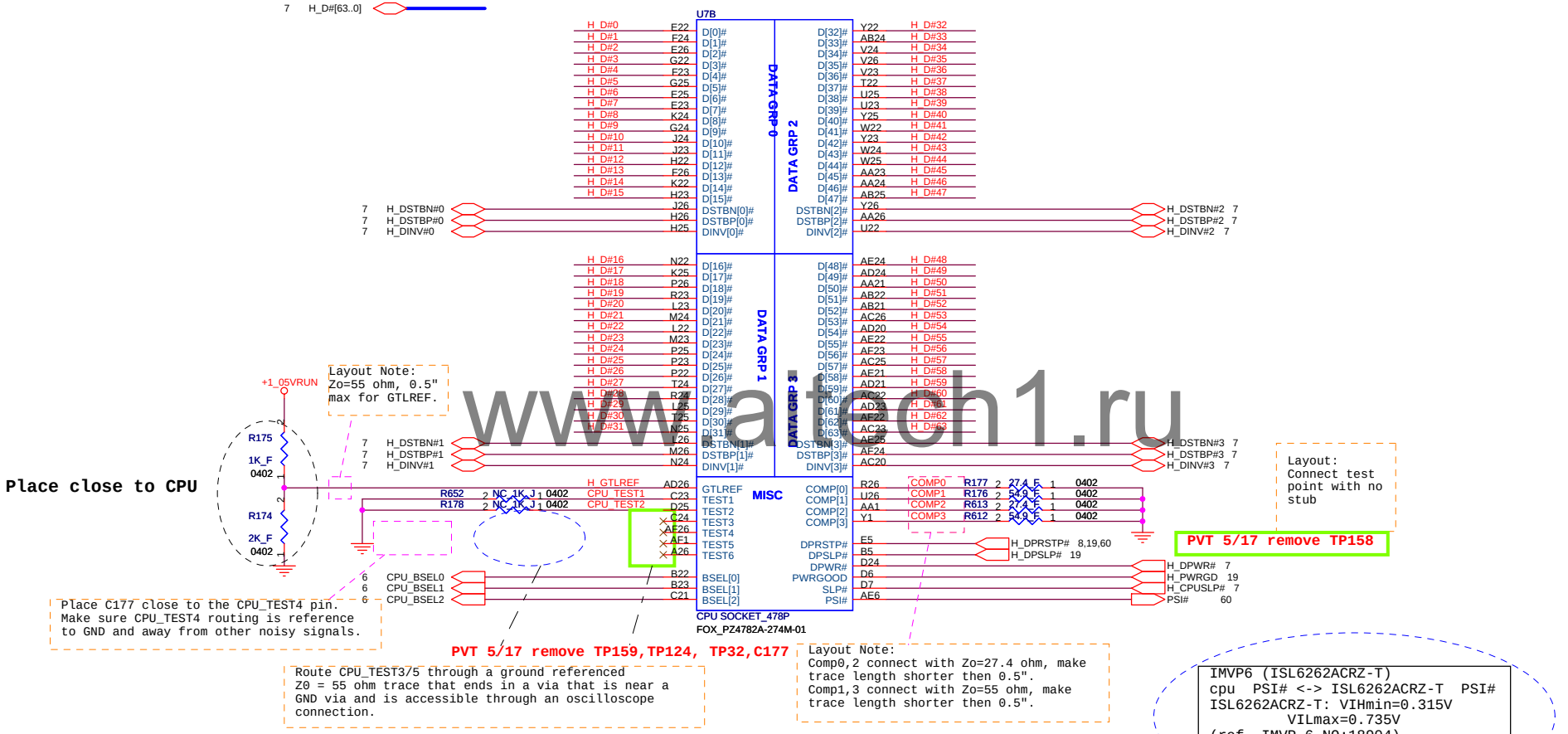

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	266MHz
L L H	133MHz
L H H	166MHz
L H L	200MHz
H H L	400MHz
H H H	Reserve
H L H	100MHz
H L L	333MHz

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Title: *Merom (HOST BUS) 2/3*

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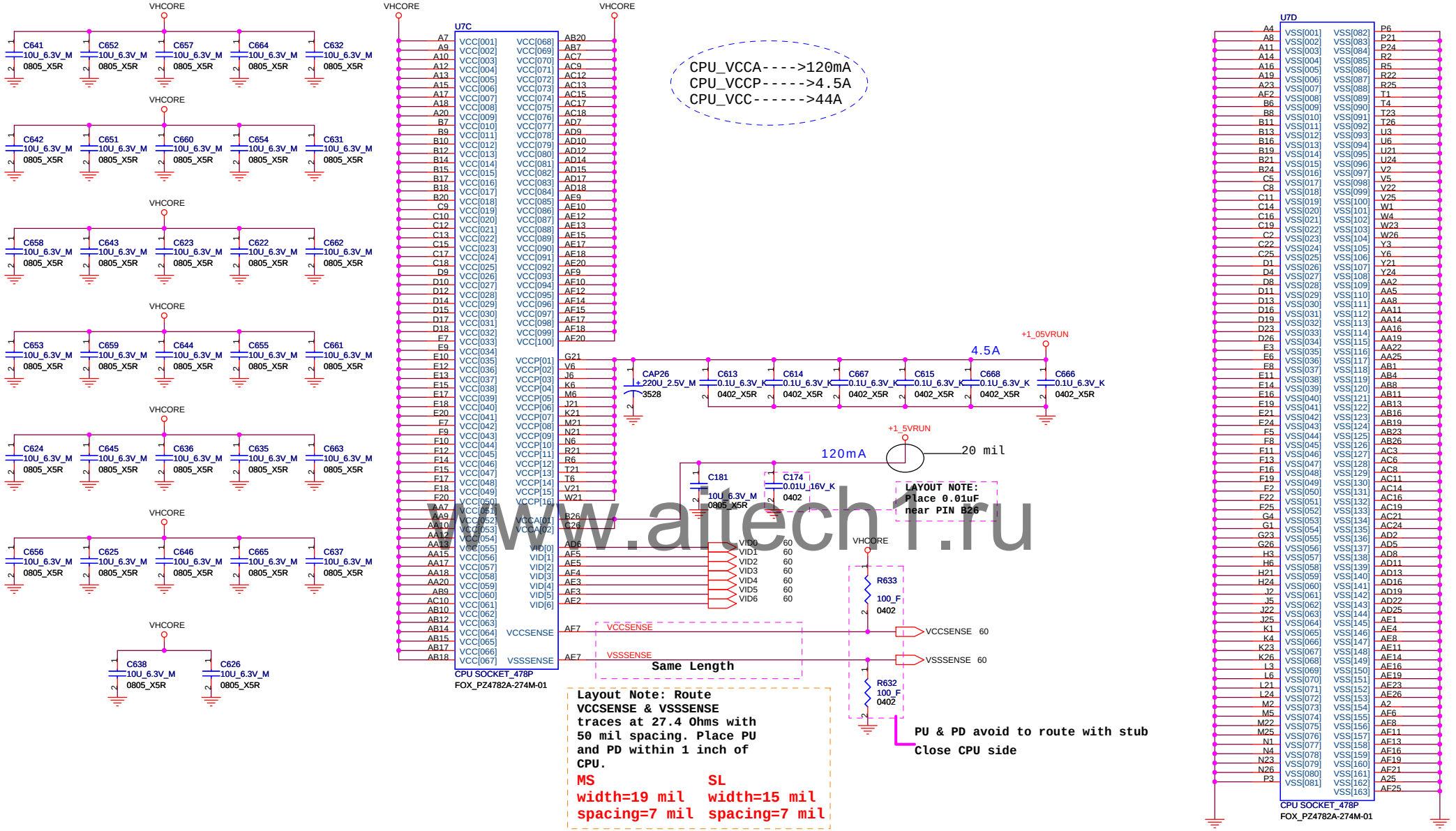

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Title: Merom (POWER/GROUND) 3/3

Size: A3 | Document Number: M630/M640 | Rev: SA

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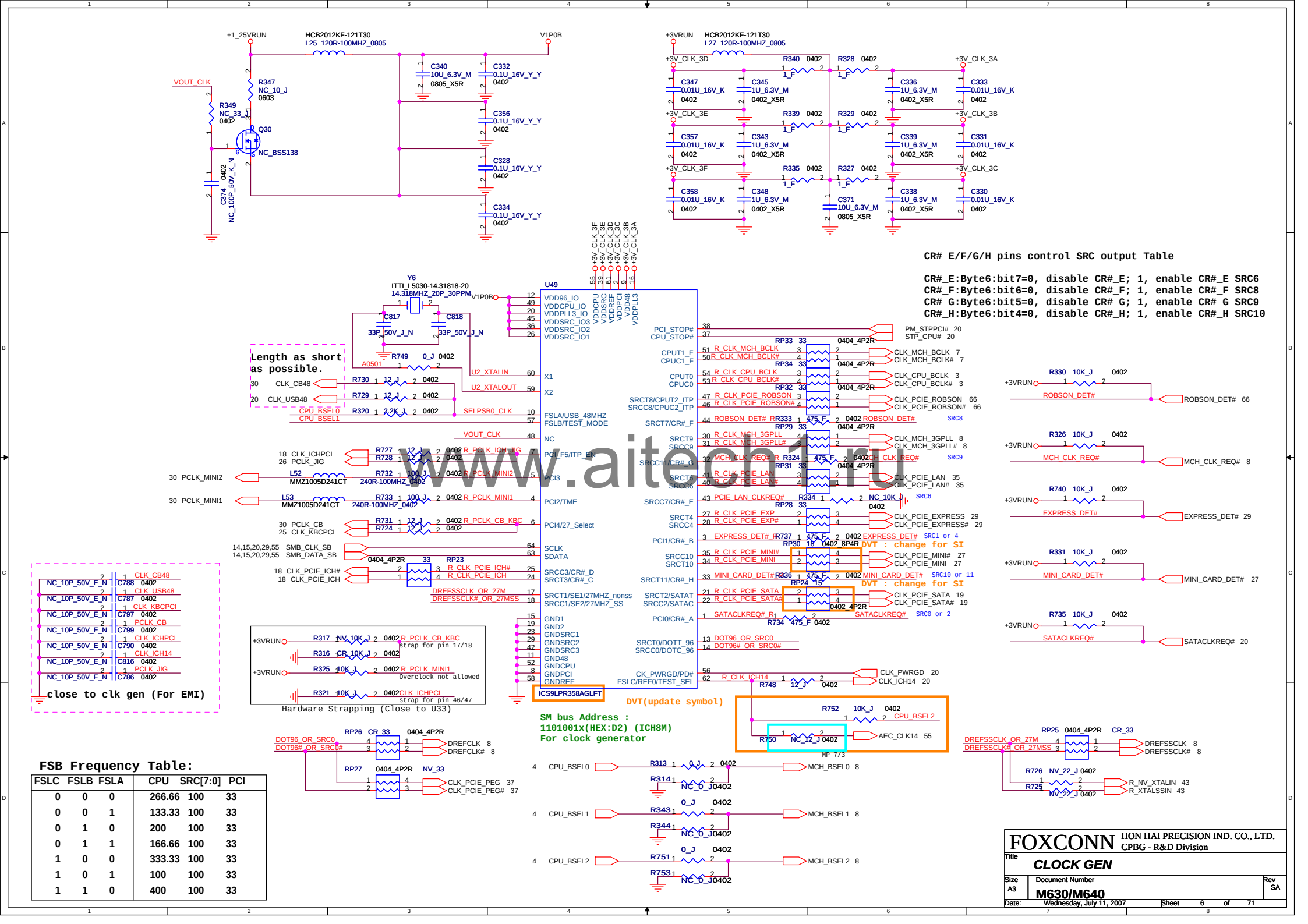

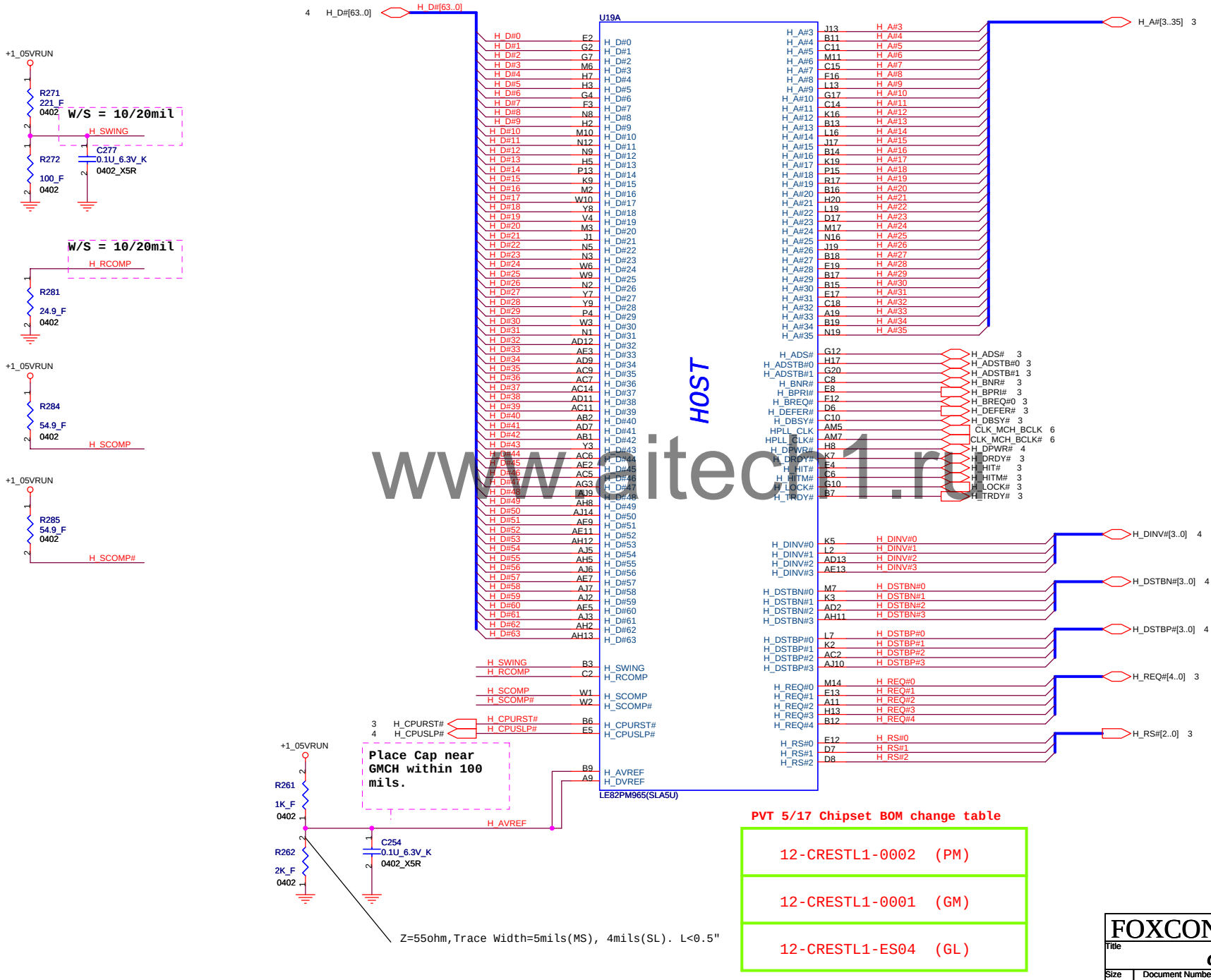

PVT 5/17 Chipset BOM change table

12-CRESTL1-0002 (PM)
12-CRESTL1-0001 (GM)
12-CRESTL1-ES04 (GL)

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Title: *Crestline (HOST) 1/of 7*

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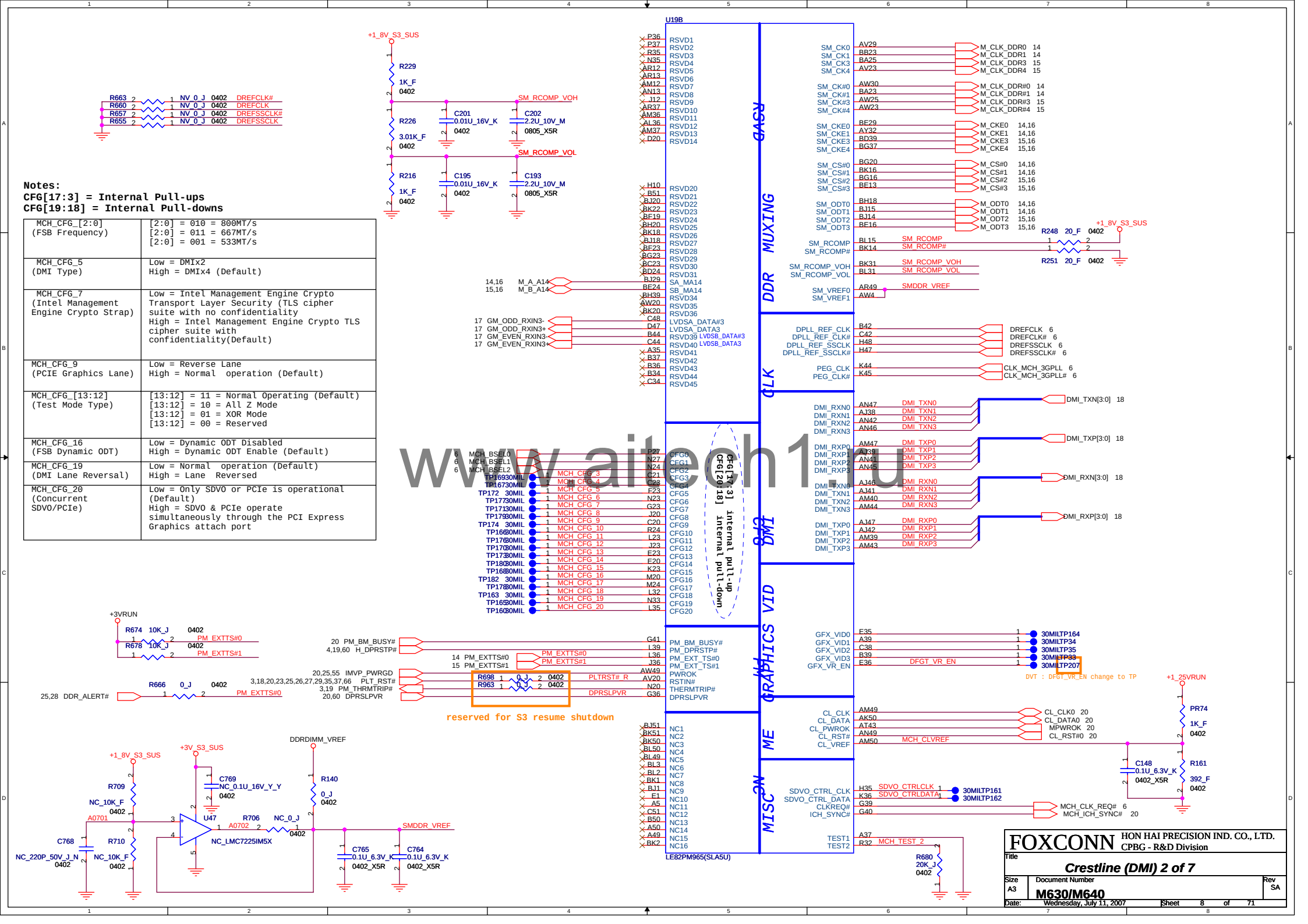
Notes:
CFG[17:3] = Internal Pull-ups
CFG[19:18] = Internal Pull-downs
MCH_CFG_[2:0] (FSB Frequency) | [2:0] = 010 = 800MT/s; [2:0] = 011 = 667MT/s; [2:0] = 001 = 533MT/s
MCH_CFG_5 (DMI Type) | Low = DMIx2; High = DMIx4 (Default)
MCH_CFG_7 (Intel Management Engine Crypto Strap) | Low = Intel Management Engine Crypto Transport Layer Security (TLS cipher suite with no confidentiality; High = Intel Management Engine Crypto TLS cipher suite with confidentiality(Default)
MCH_CFG_9 (PCIE Graphics Lane) | Low = Reverse Lane; High = Normal operation (Default)
MCH_CFG_[13:12] (Test Mode Type) | [13:12] = 11 = Normal Operating (Default); [13:12] = 10 = All Z Mode; [13:12] = 01 = XOR Mode; [13:12] = 00 = Reserved
MCH_CFG_16 (FSB Dynamic ODT) | Low = Dynamic ODT Disabled; High = Dynamic ODT Enable (Default)
MCH_CFG_19 (DMI Lane Reversal) | Low = Normal operation (Default); High = Lane Reversed
MCH_CFG_20 (Concurrent SDVO/PCIe) | Low = Only SDVO or PCIe is operational (Default); High = SDVO & PCIe operate simultaneously through the PCI Express Graphics attach port
U19B
LE82PM965(SLA5U)
CFG[17:3] internal pull-up
CFG[20:18] internal pull-down
reserved for S3 resume shutdown
DVT : DFGT_VR_EN change to TP
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Crestline (DMI) 2 of 7
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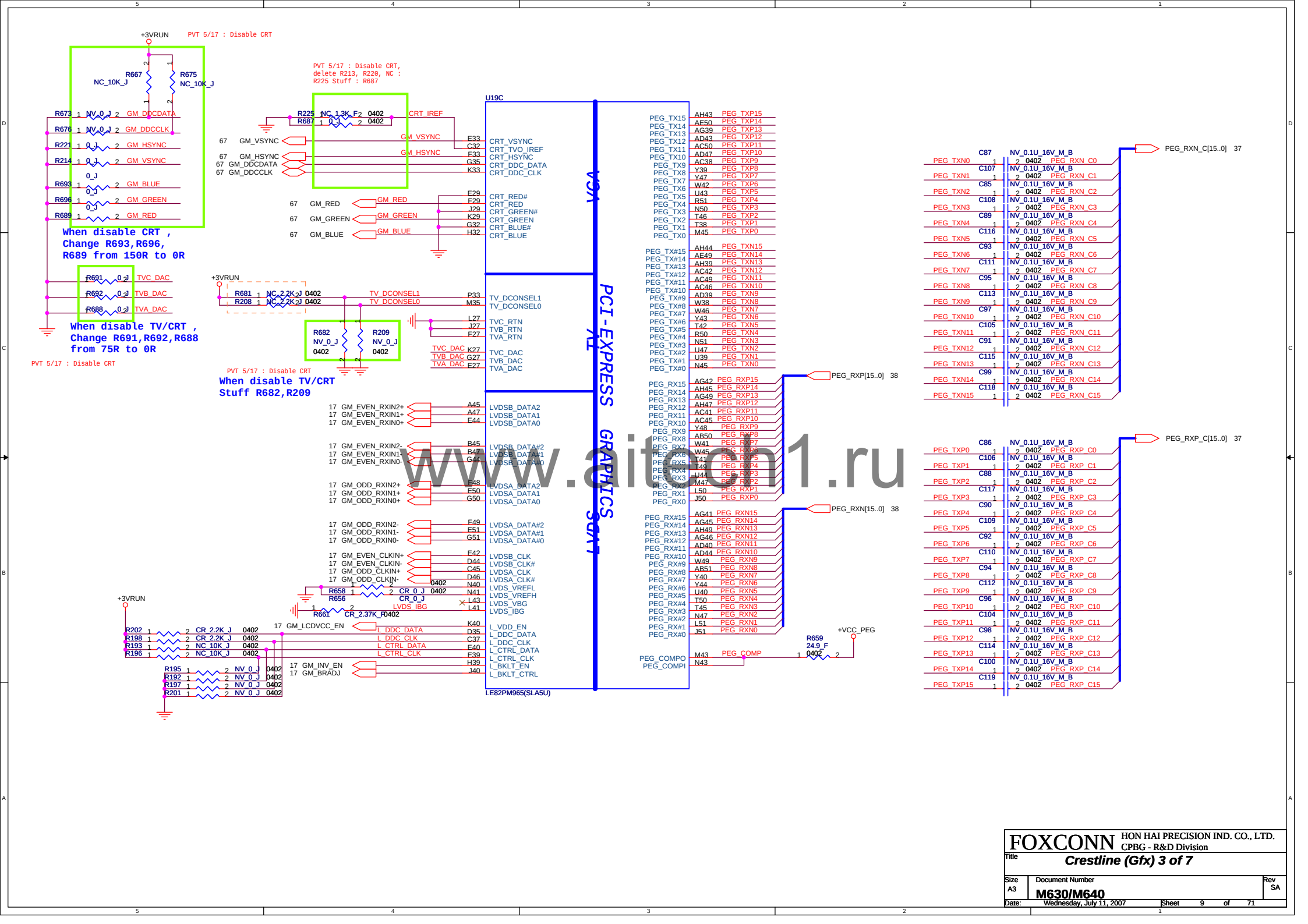

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Crestline (DDRII) 4 of 7
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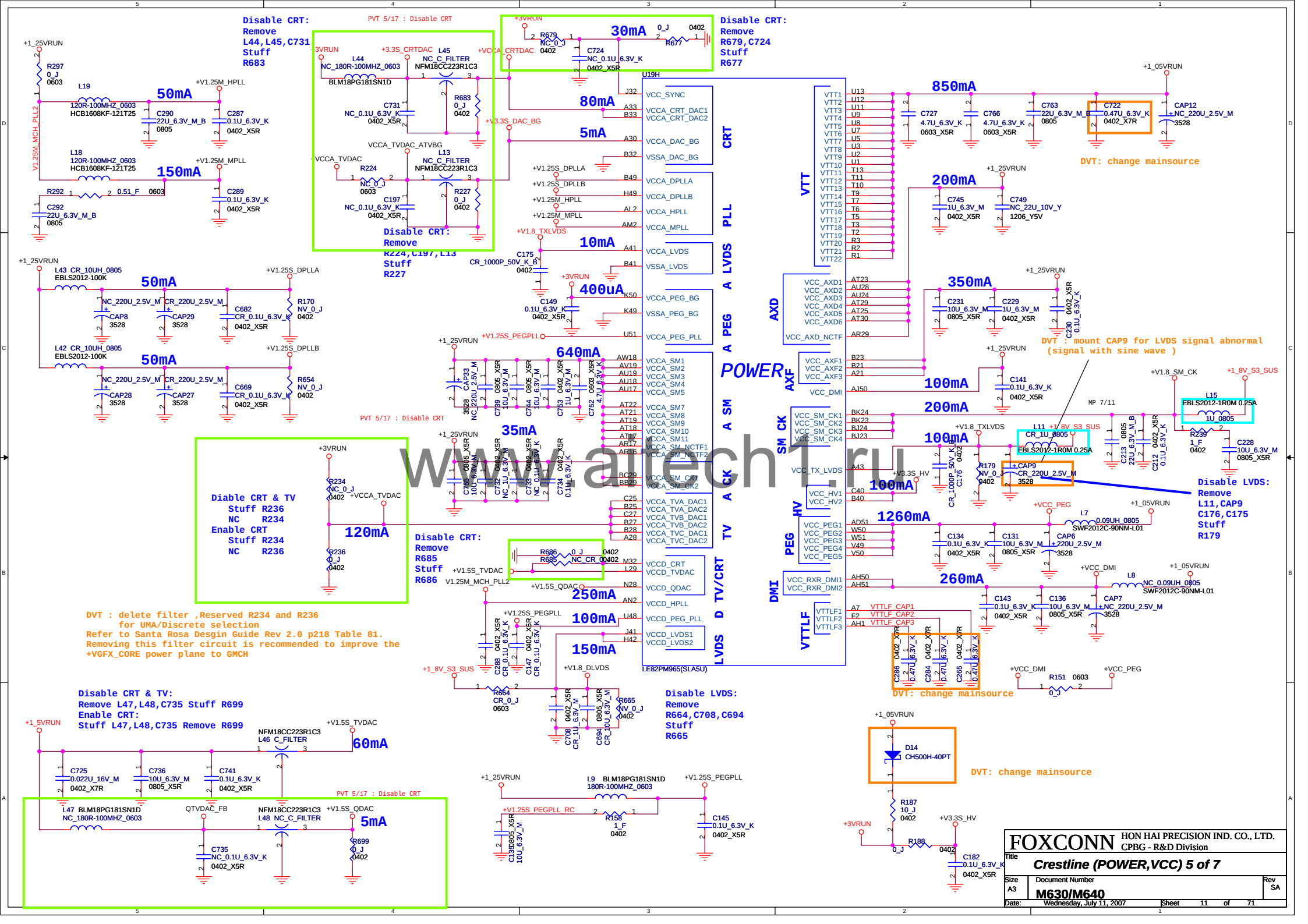

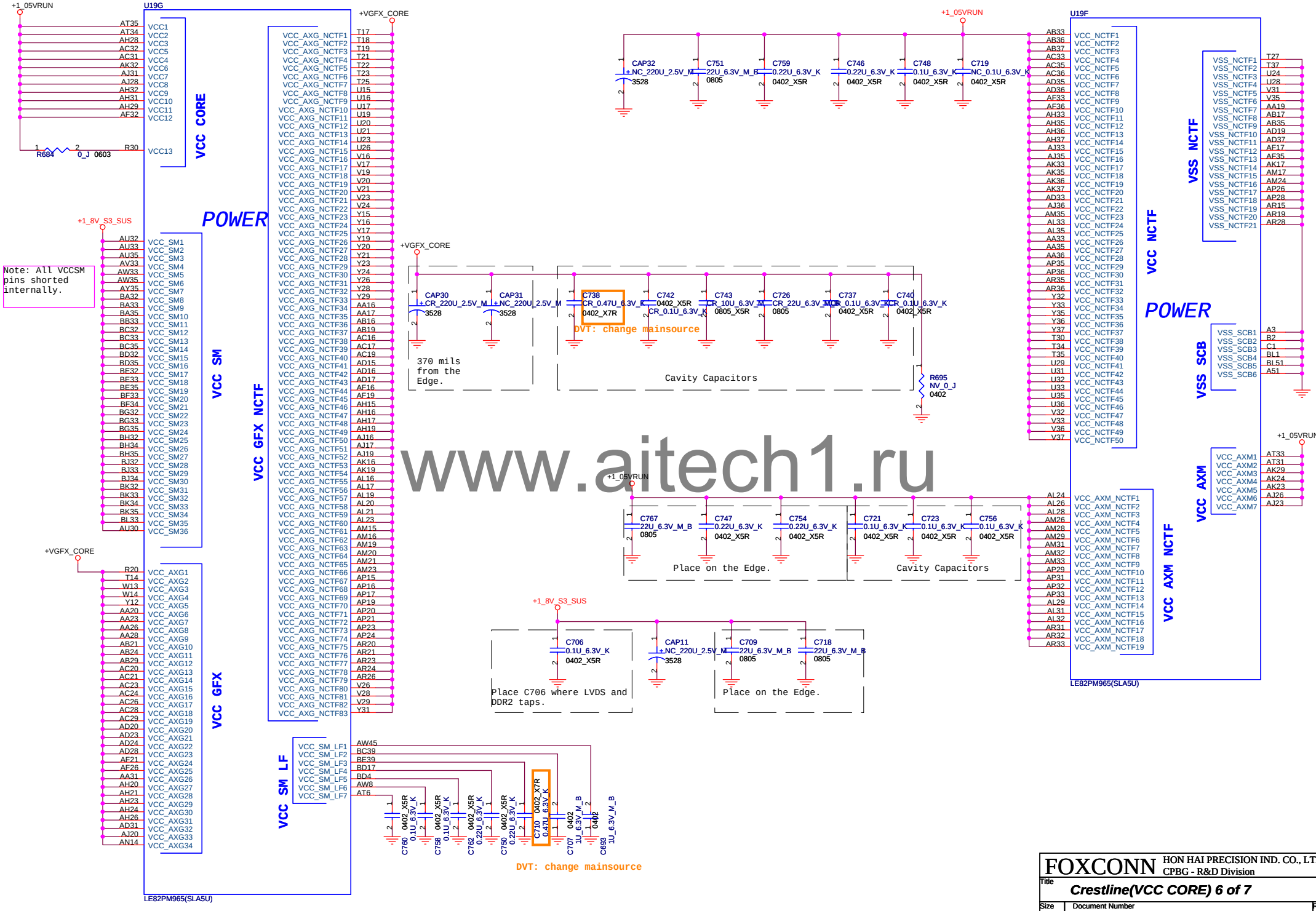

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Crestline(VCC CORE) 6 of 7
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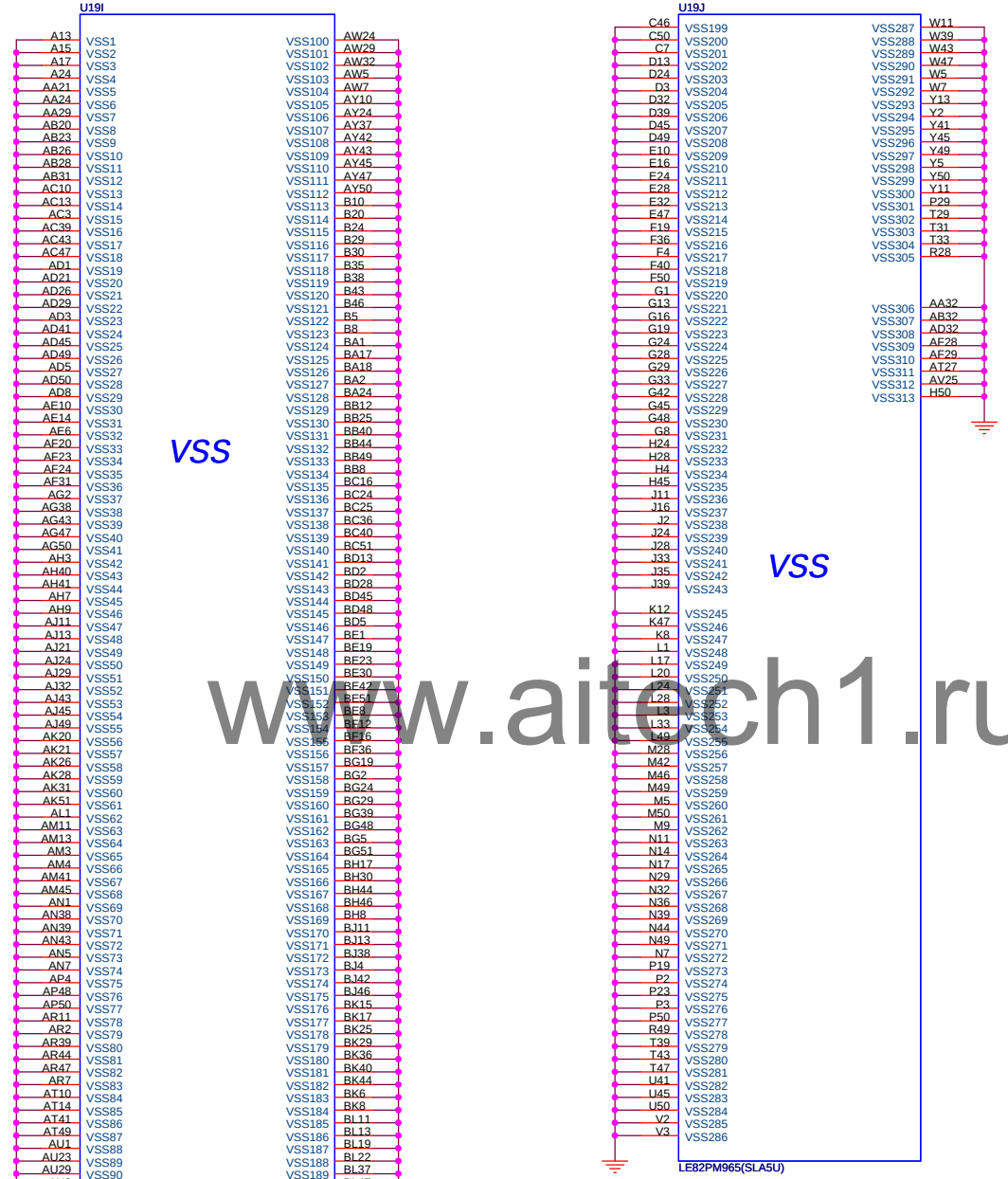

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*Crestline (VSS) 7 of 7*	
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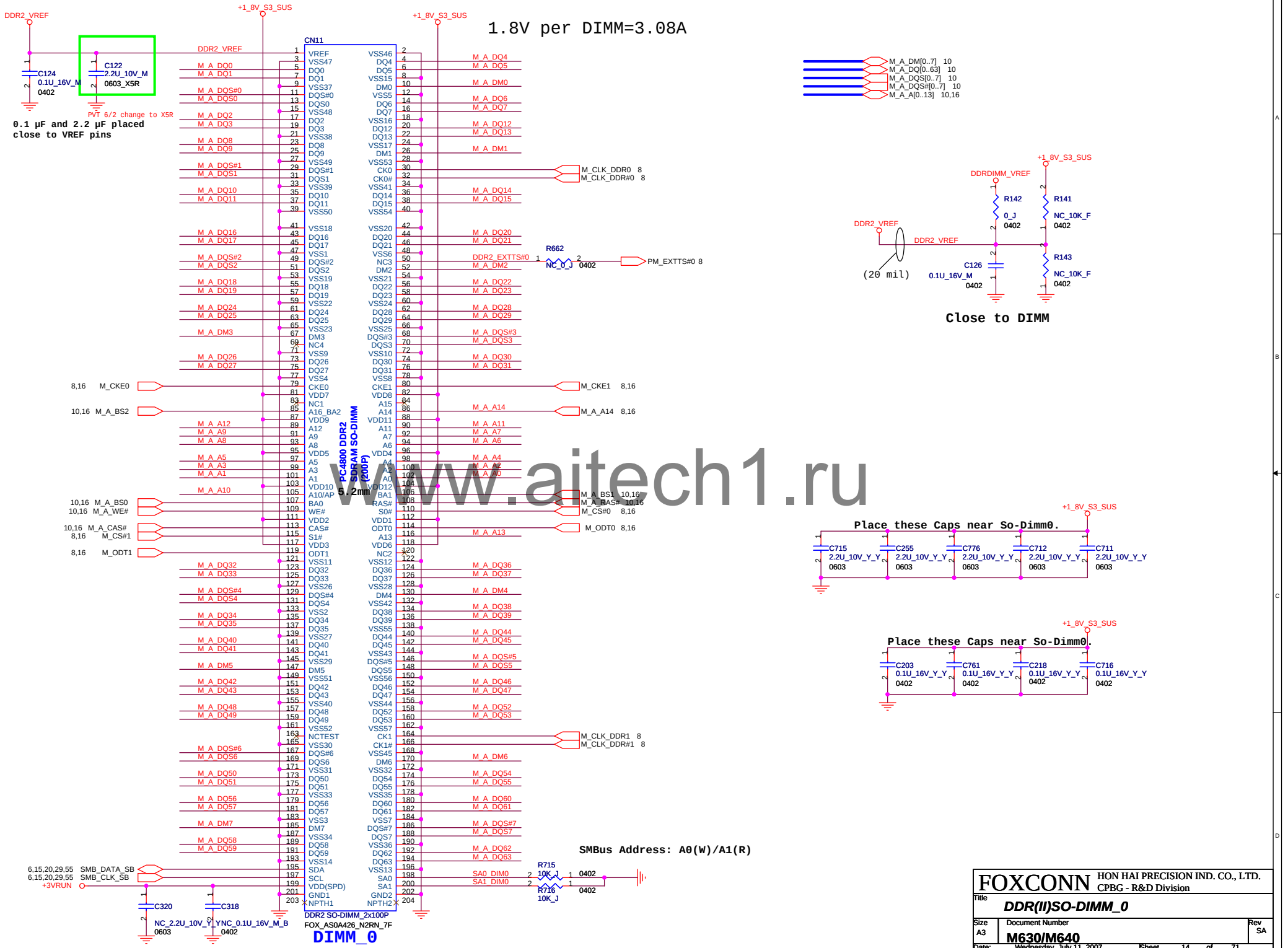
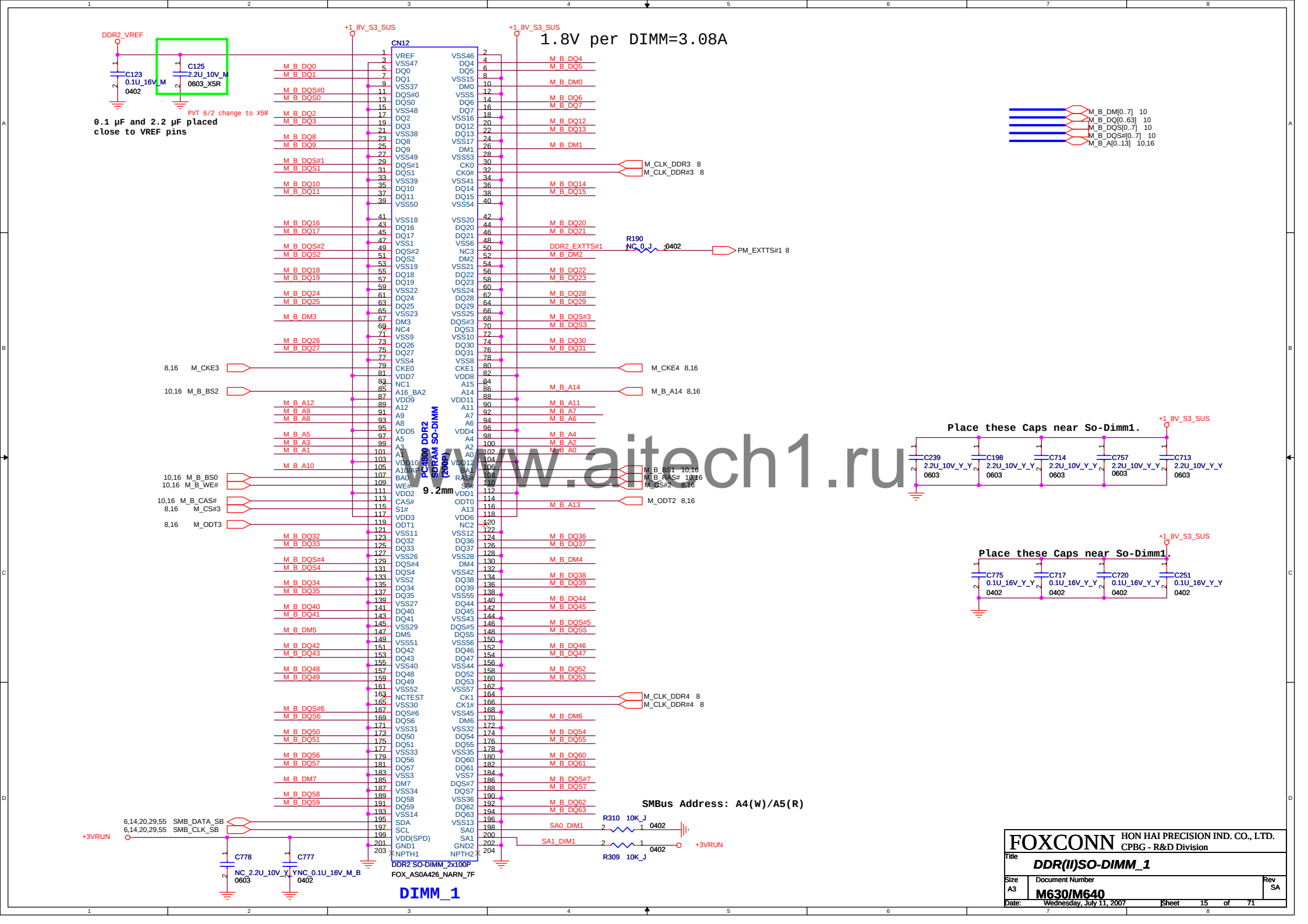
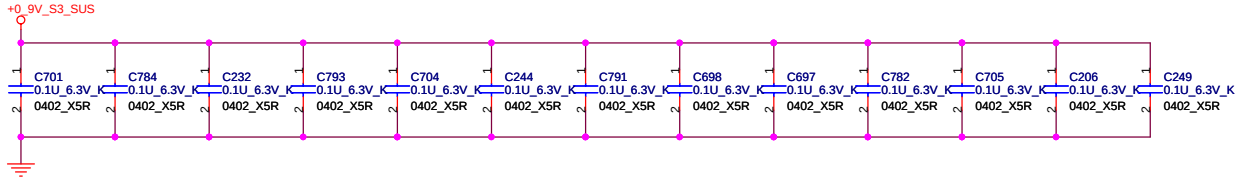
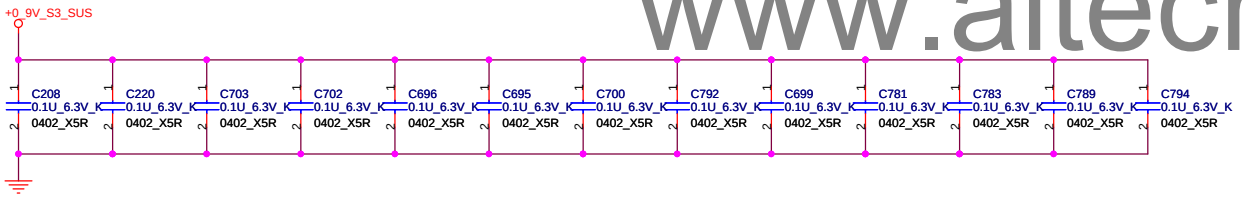


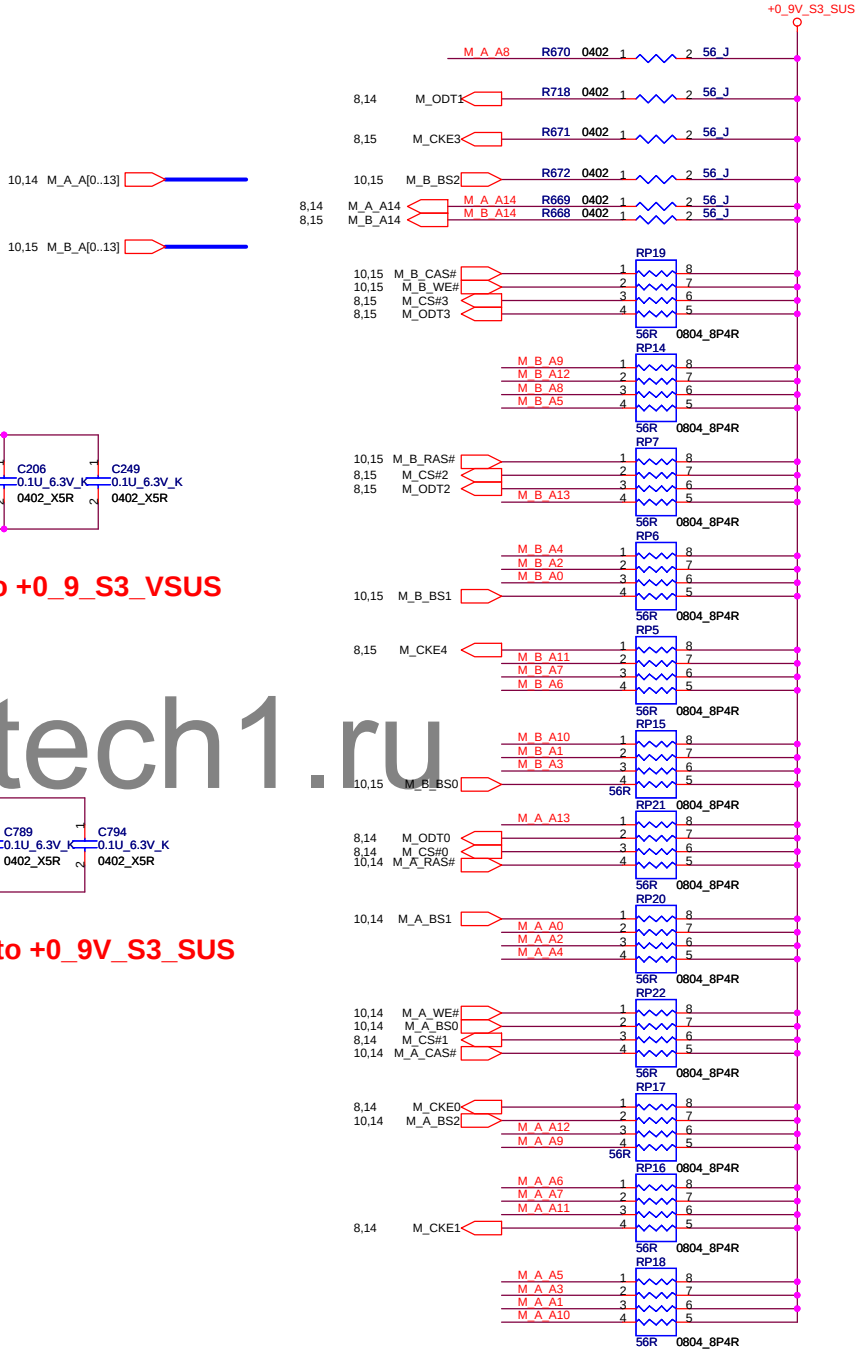




Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9_S3_VSUS



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9V_S3_SUS



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: ***DDR(II)Termination***		
Size: A3	Document Number: **M630/M640**	Rev: SA
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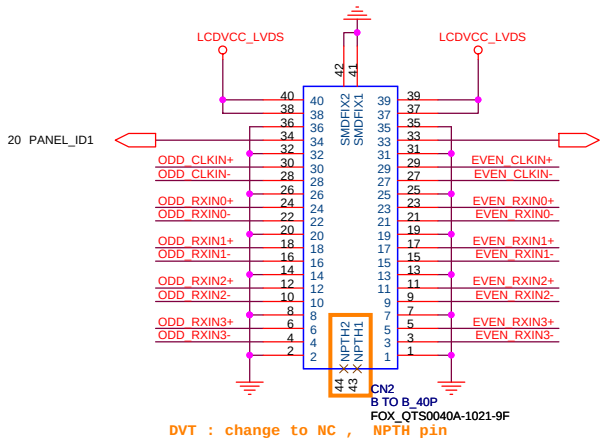
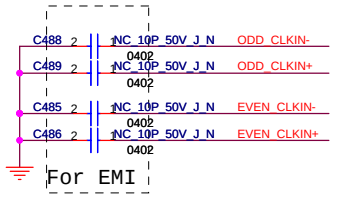
LVDS



DVT : change to NC , NPTH pin

LVDS CONNECTOR

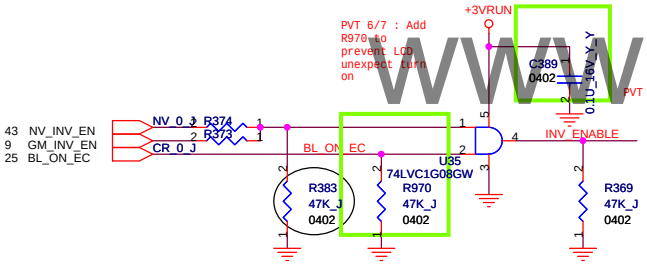


M630, 19"

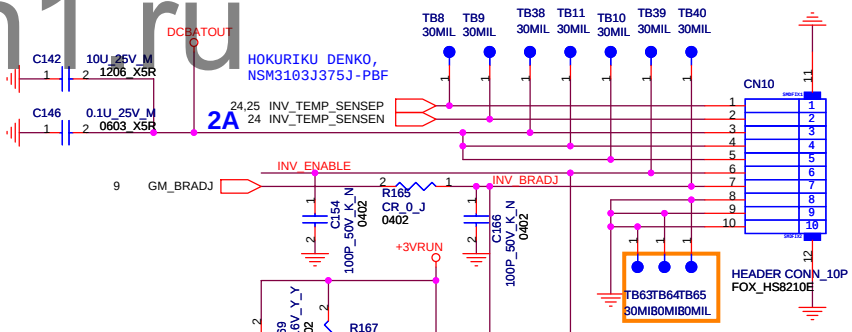
	Type 1	Type 2	Type 3	Type 4
00	AUO M190PW01 V.1			V
01			V	
10		V		
11				

M640, 22"

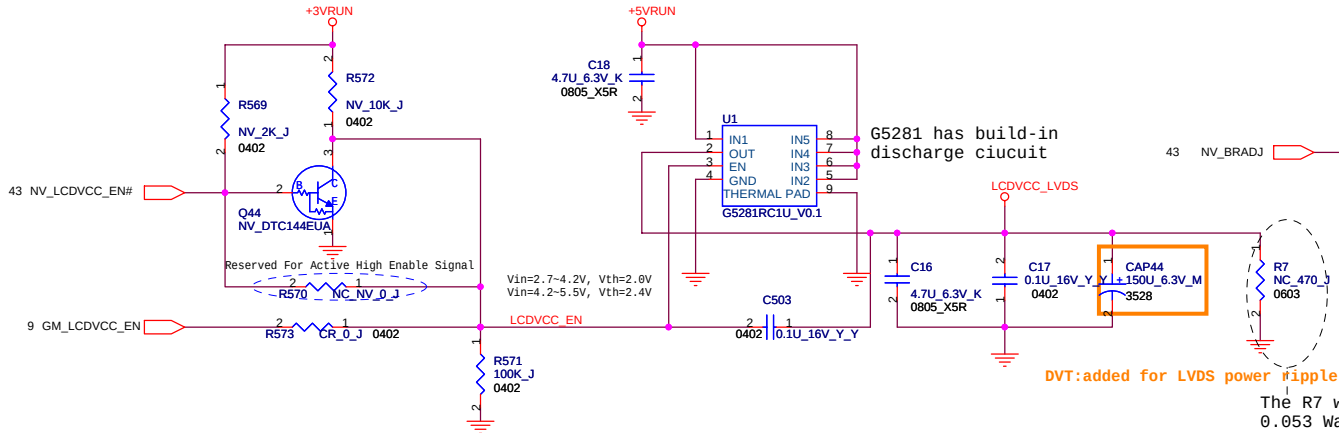
	Type 1	Type 2	Type 3	Type 4
00	AUO M220EW01 V.2			V
01			V	
10		V		
11				



NVIDIA FAE SUGGESTS TO ADD PULL DOWN RESISTOR



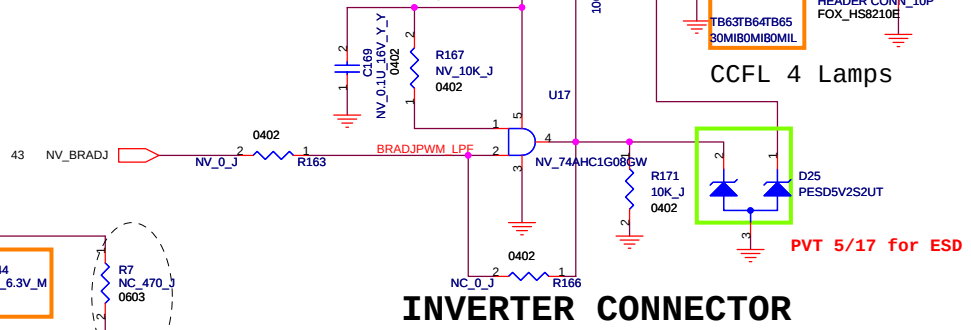
CCFL 4 Lamps



DVT:added for LVDS power ripple (too large,spec is 200mv)

The R7 will consume about 0.053 Watt (5x5/470 = 0.053W). We changed resistor to 0603 size (1/10 Watt)

LCD POWER



PVT 5/17 for ESD

INVERTER CONNECTOR

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
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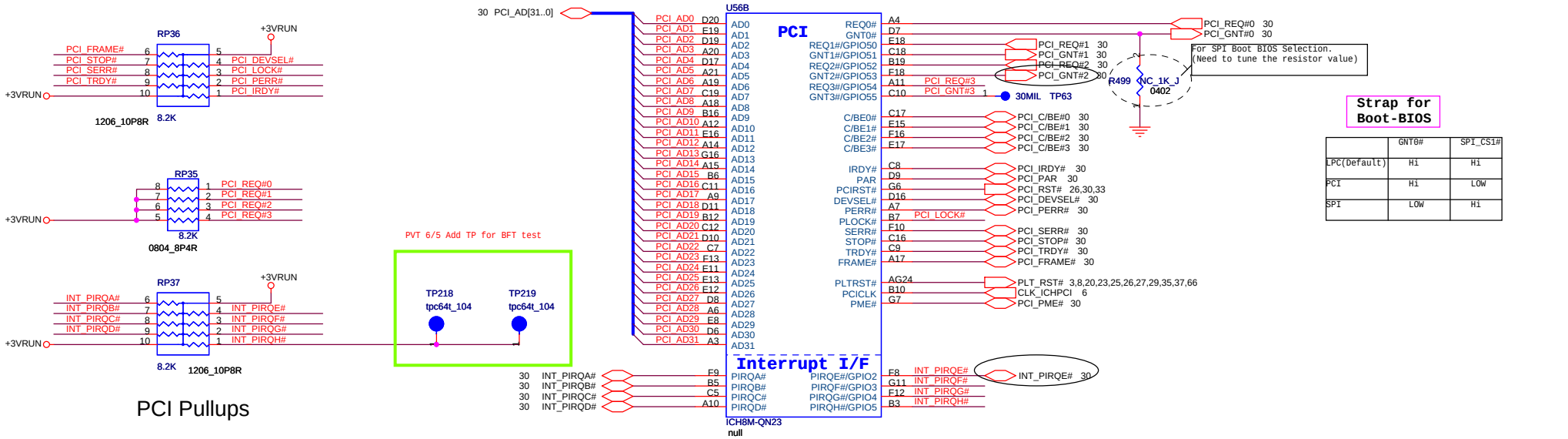

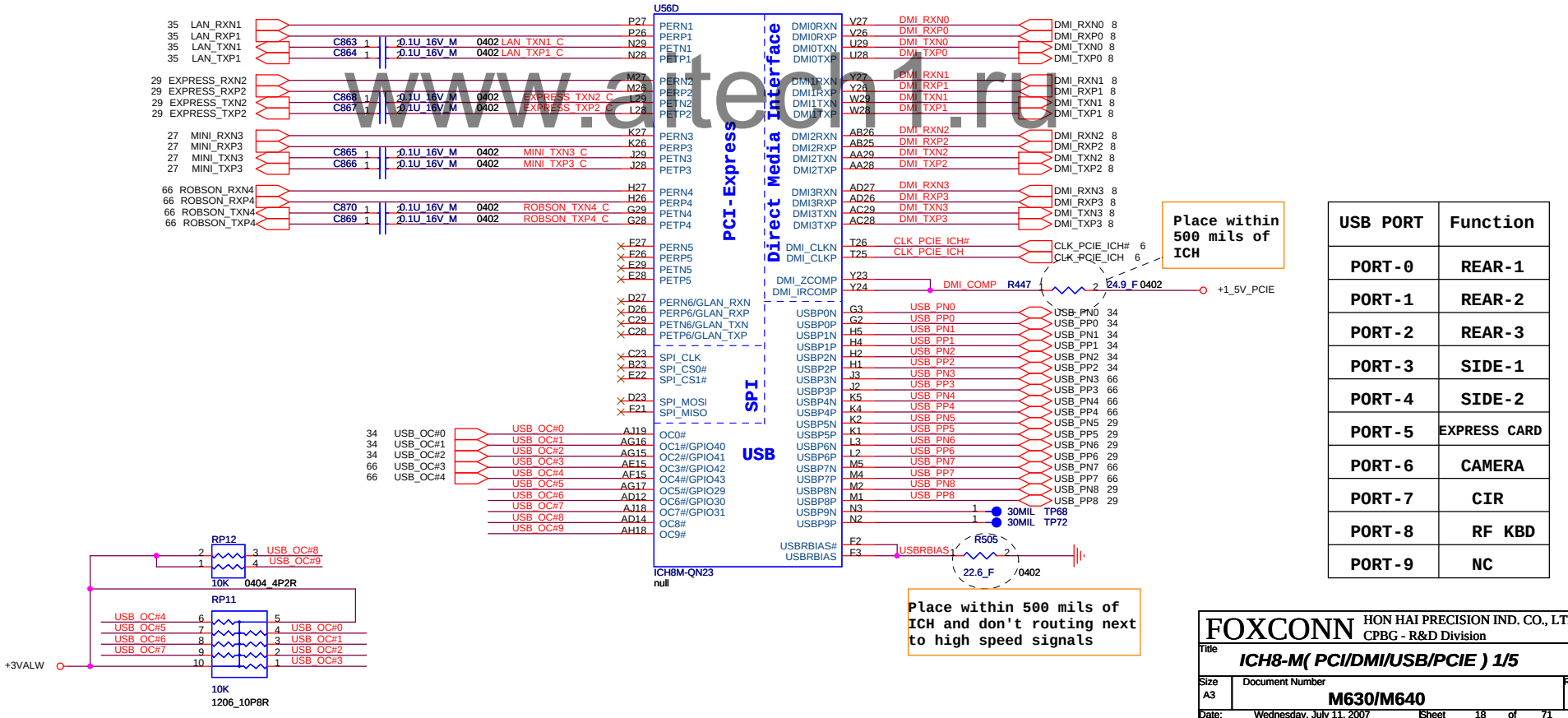

USB PORT	Function
PORT-0	REAR-1
PORT-1	REAR-2
PORT-2	REAR-3
PORT-3	SIDE-1
PORT-4	SIDE-2
PORT-5	EXPRESS CARD
PORT-6	CAMERA
PORT-7	CIR
PORT-8	RF KBD
PORT-9	NC

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Title: ICH8-M(PCI/DMI/USB/PCIE) 1/5

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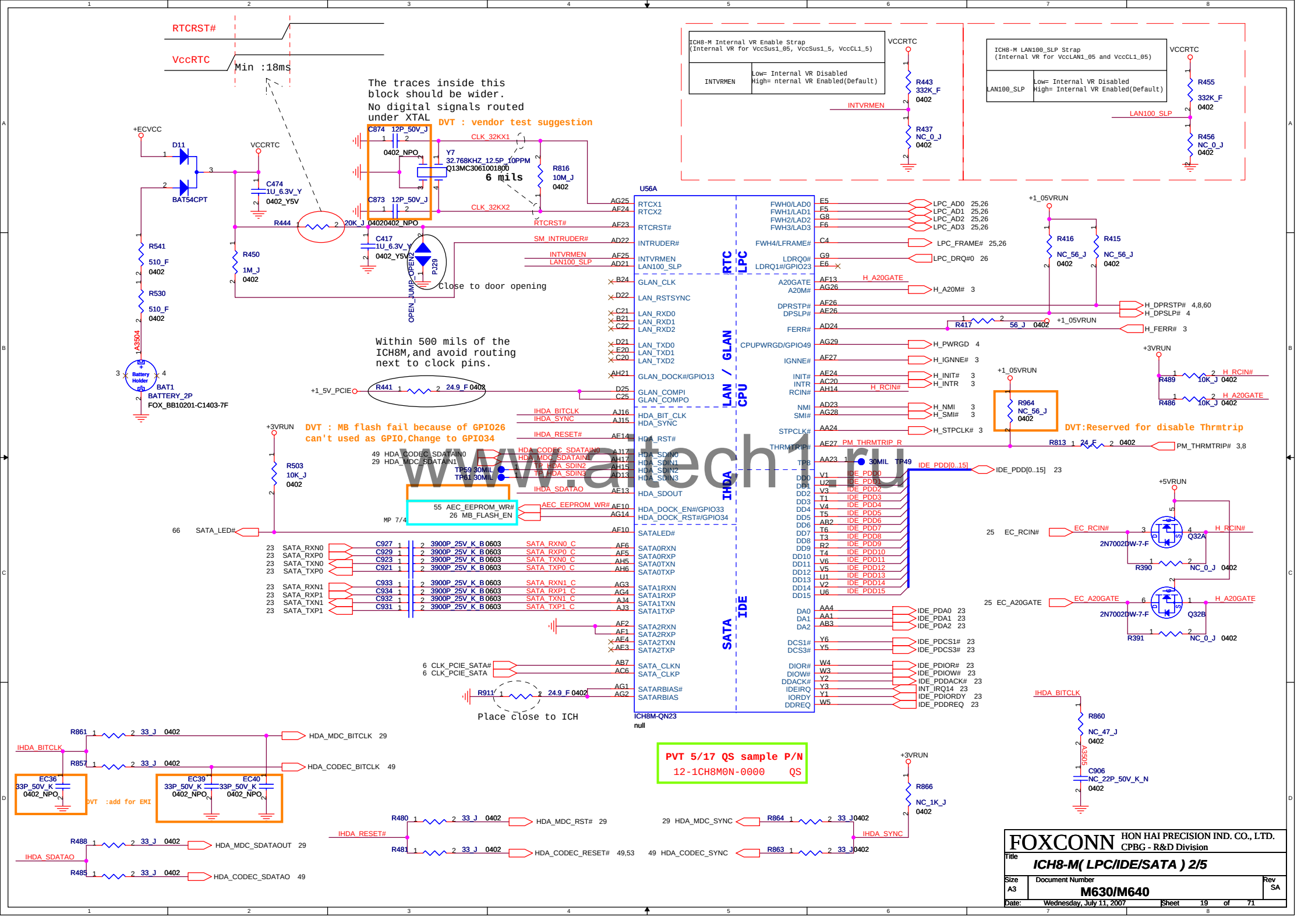
RTCRST#
VccRTC
Min :18ms
The traces inside this block should be wider.
No digital signals routed under XTAL
DVT : vendor test suggestion
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5, VccCL1_5)
INTVRMEN
Low= Internal VR Disabled
High= nternal VR Enabled(Default)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
LAN100_SLP
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
Close to door opening
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
DVT : MB flash fail because of GPIO26 can't used as GPIO,Change to GPIO34
DVT:Reserved for disable Thrmtrip
Place close to ICH
PVT 5/17 QS sample P/N
12-1CH8M0N-0000 QS
DVT :add for EMI
U56A
ICH8M-QN23
null
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH8-M(LPC/IDE/SATA) 2/5
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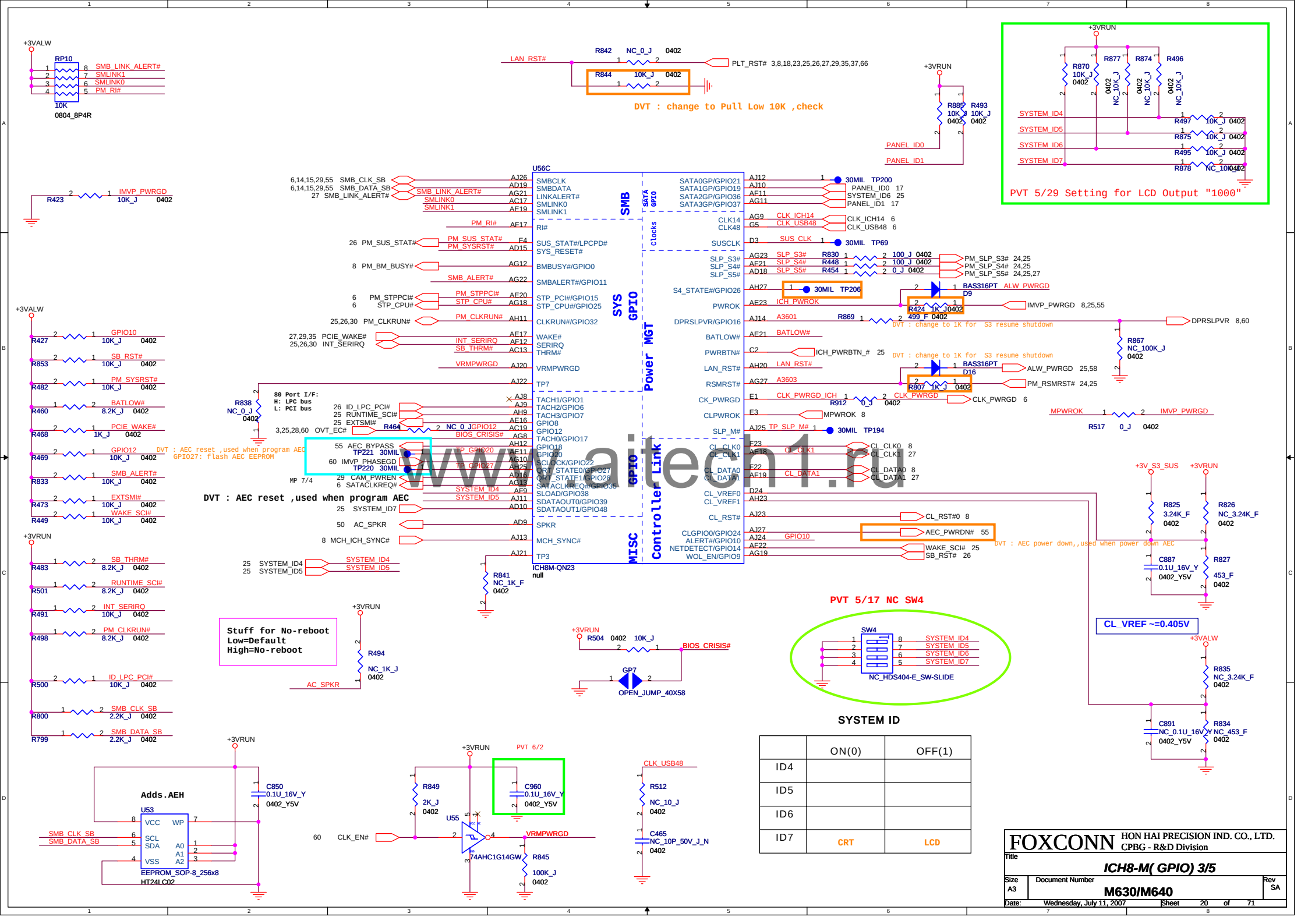

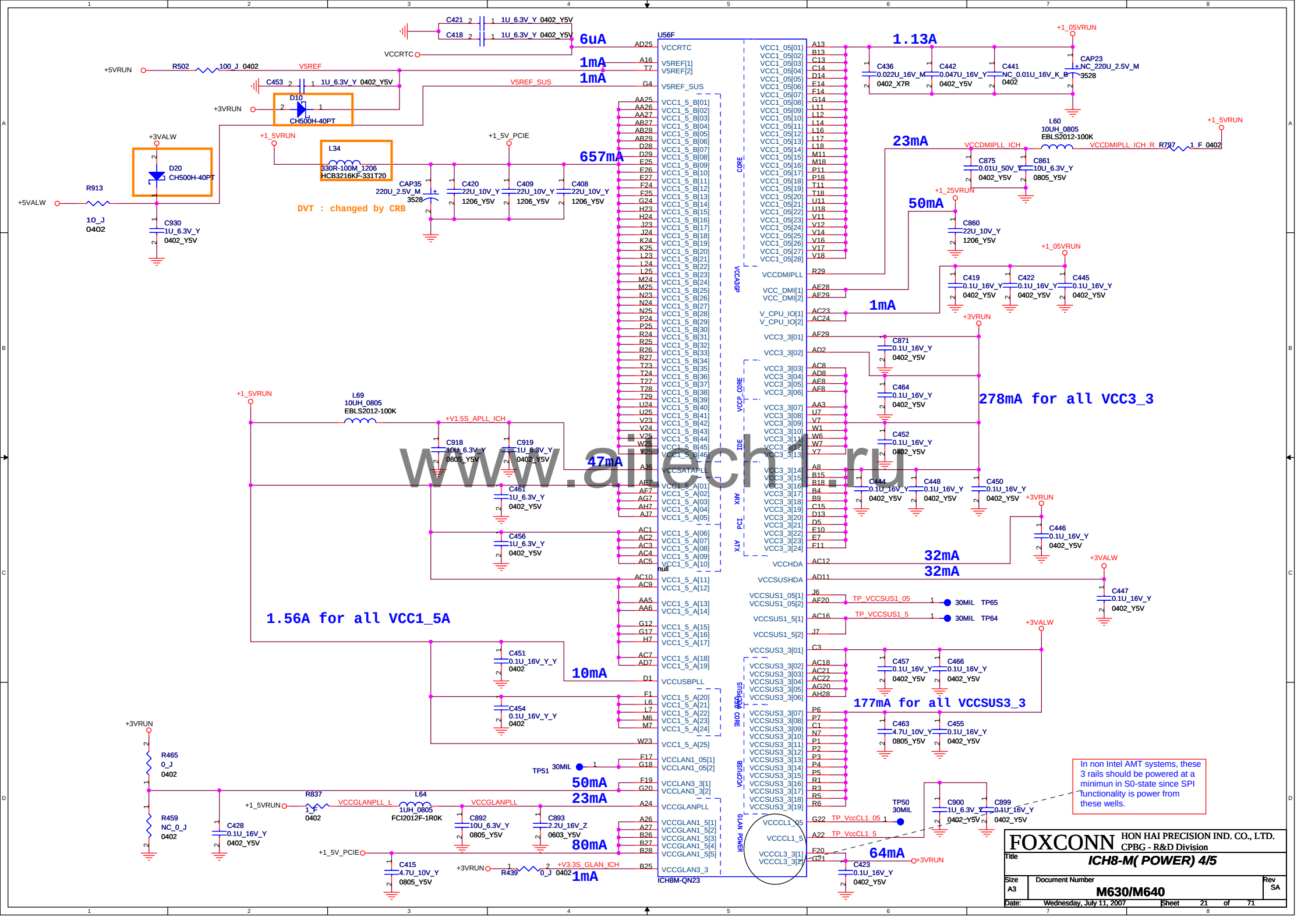

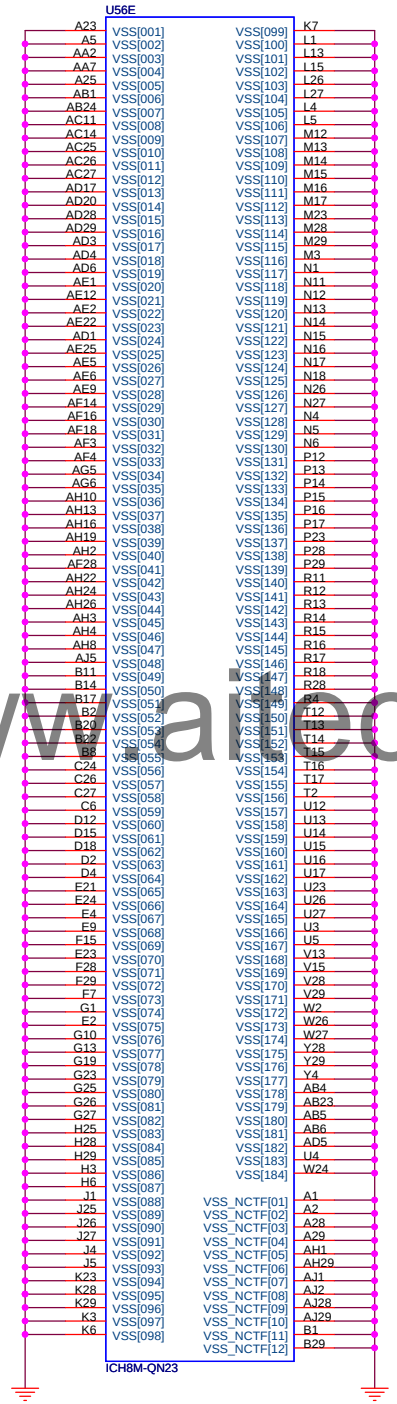

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Title: ICH8-M(GND) 5/5

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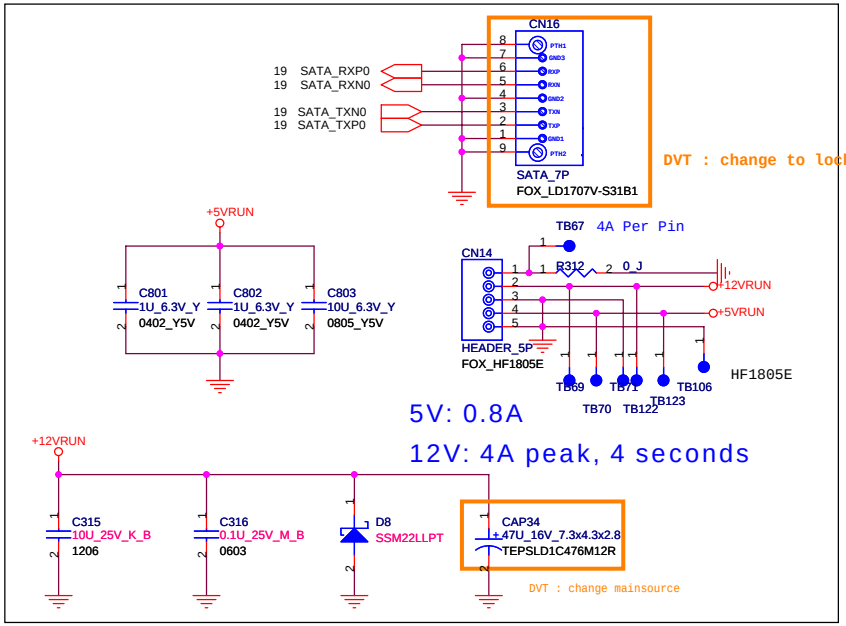
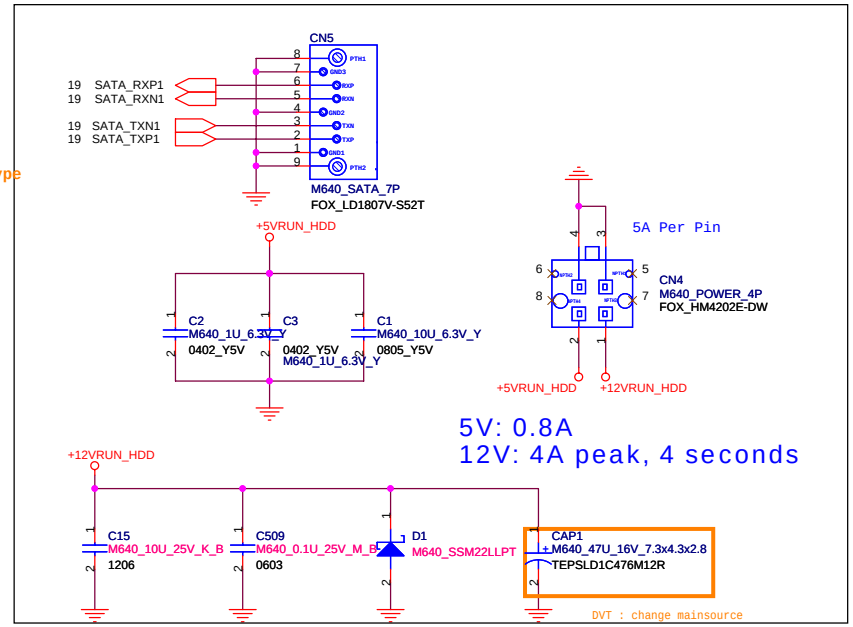
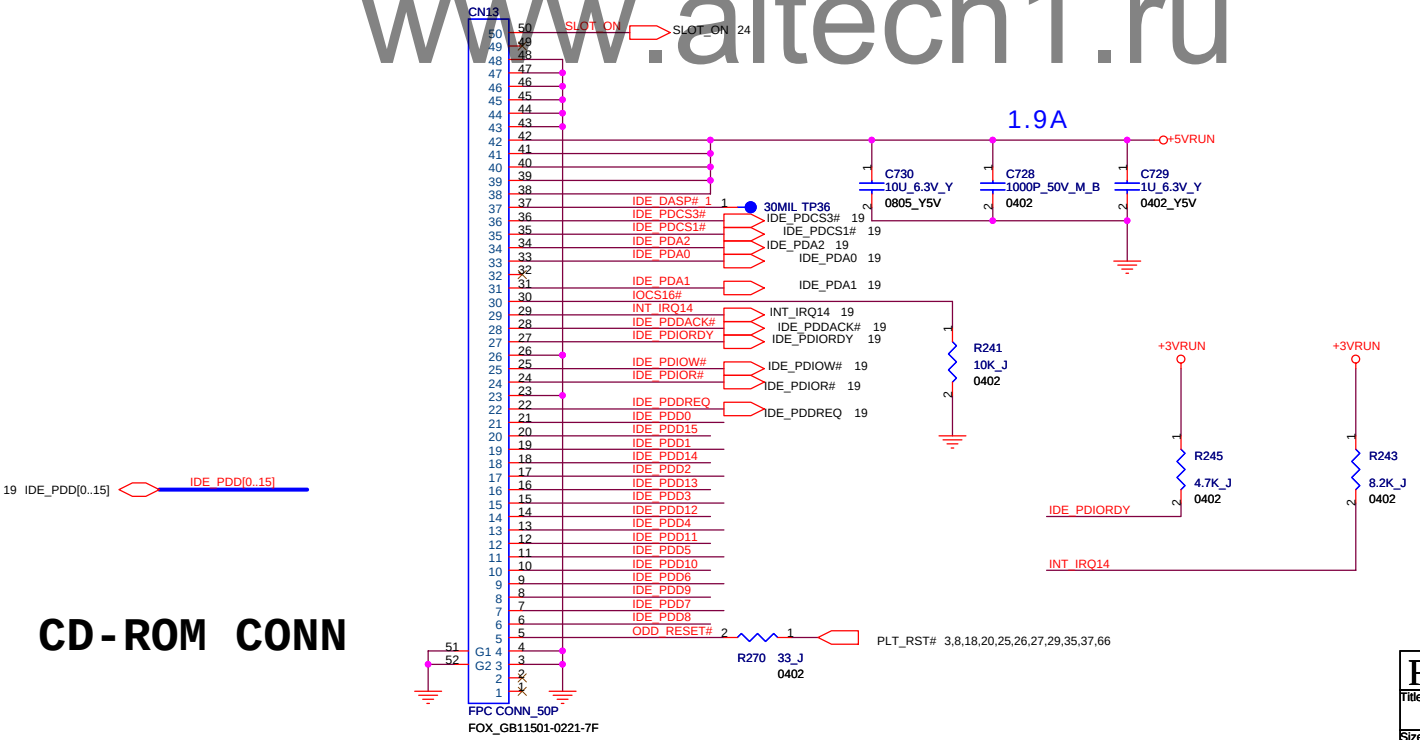
SATA HDD CONN



HDD1



HDD2



CD-ROM CONN

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	SATA HDD/CD-ROM		
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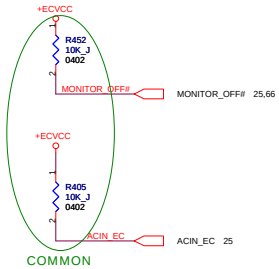
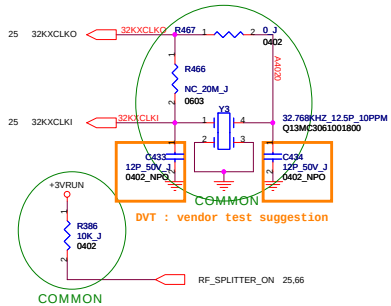
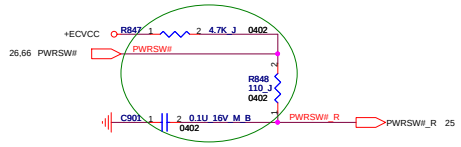


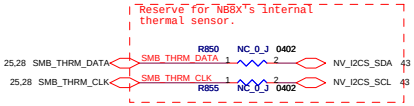
DVT : delete winbond

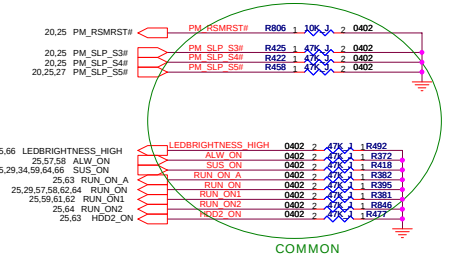


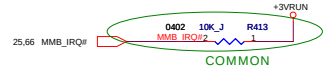
H(3.0-3.6) :RF AMP ON * default (need to pull up)
L(0) :RF AMP OFF

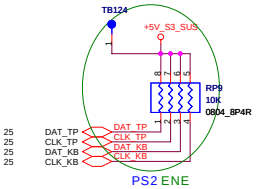
DVT :netname in 3910 don't connect

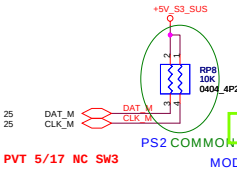




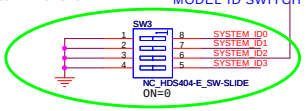








PVT 5/17 NC SW3

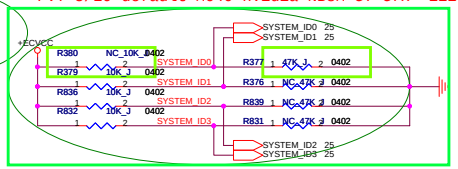


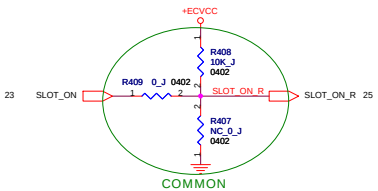
PVT 6/1 Add system ID table

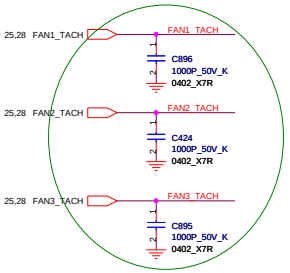
	0	1
SYSTEM_ID0	R377	R380
SYSTEM_ID1	R376	R379
SYSTEM_ID2	R839	R836
SYSTEM_ID3	R831	R832

M630 PVT SKU	M630 8M 256H	M630 8M 128Q	M630 GM	M630 GL
SYSTEM_ID0	0	0	1	0
SYSTEM_ID1	1	1	0	0
SYSTEM_ID2	0	0	0	0
SYSTEM_ID3	1	1	1	1
M640 PVT SKU	M640 8M 256Q	M640 8M 128H	M640 GM	
SYSTEM_ID0	0	0	1	
SYSTEM_ID1	1	1	0	
SYSTEM_ID2	1	1	1	
SYSTEM_ID3	1	1	1	

PVT 5/29 default M640 nVidia NB8M-GT Gfx "1110"







JTAG Select Configuration

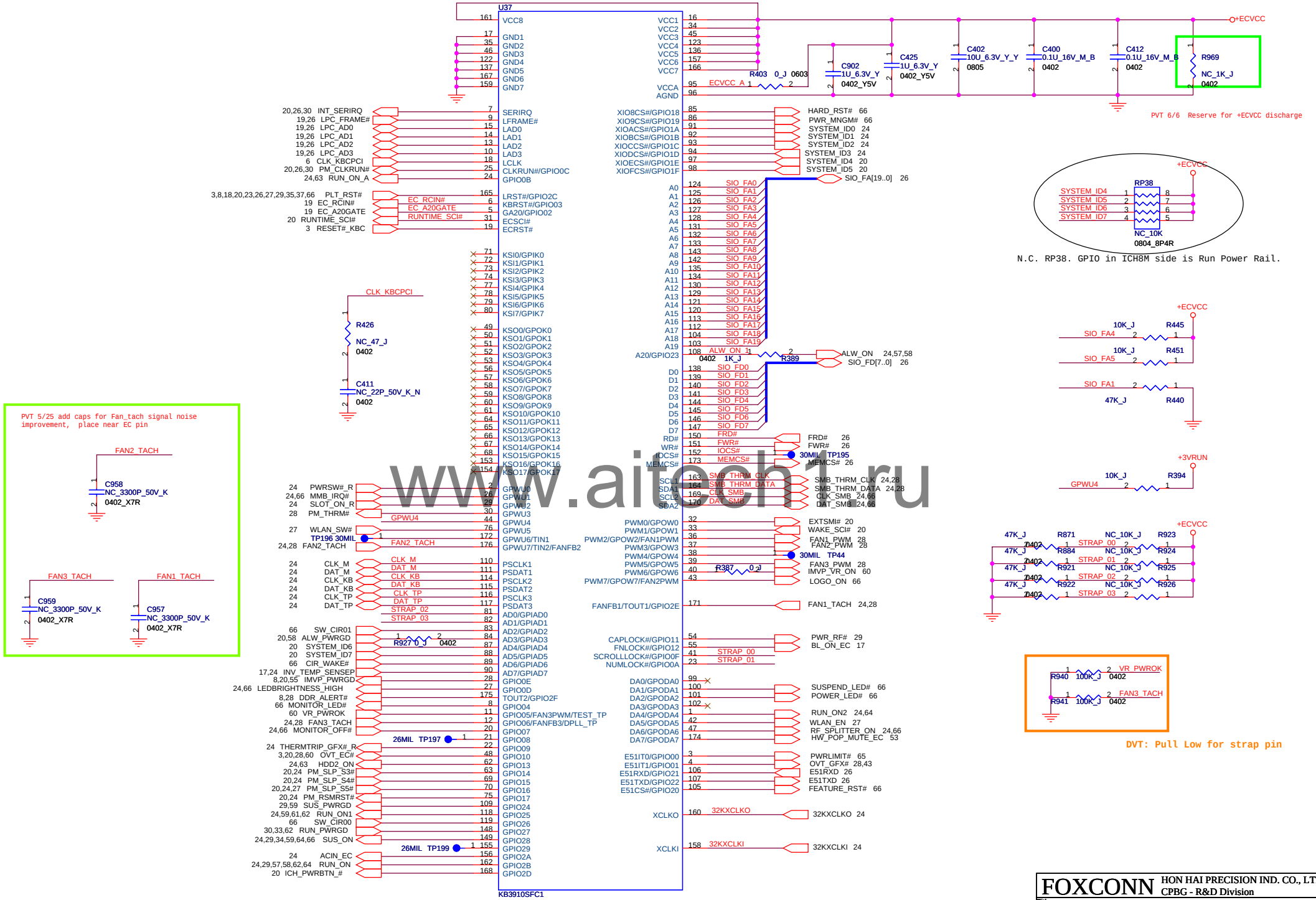
JEN0#(Pin24)	JENK#(Pin53)	Pins 17,20,21, 23,25,27	Pins 47,48,50 51,52
No power-down resistor		GPIO port signals	Keyboard scan out
Add 10K pull down	No pull down	JTAG signals	Keyboard scan out
No pull down	Add 10K pull down	GPIO port signals	JATG signals
Add 10K pull down		IIIegal Srap Combination	

SYSTEM ID Table		
ID1	ID0	Graphics Chip
0	0	Intel GL960
0	1	Intel GM965
1	0	nVidia NB8M-GT Gfx
1	1	nVidia NB8P-GS Gfx

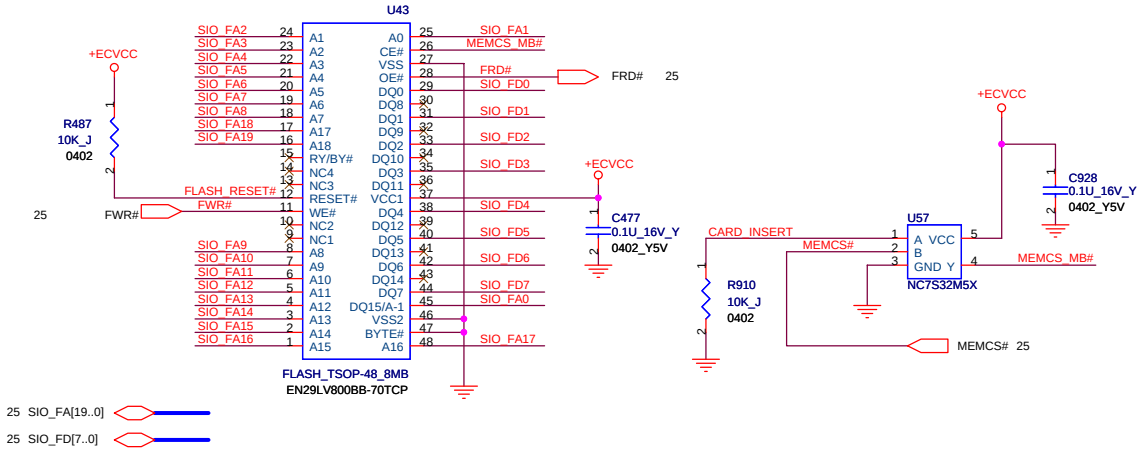
SYSTEM ID Table		
ID3	ID2	Model Name
0	0	Reserved
0	1	M620
1	0	M630
1	1	M640

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	EC(KB3925)	
Size: Custom	Document Number: M630/M640	Rev: 0.1
Date: Wednesday, July 11, 2007	Sheet 24 of 71	



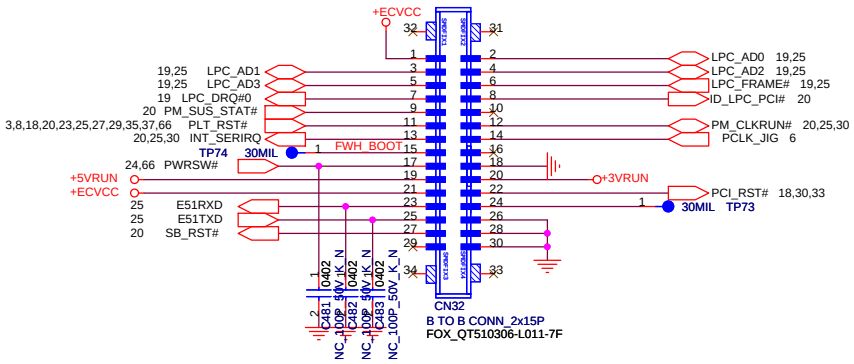
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	EC(KB3910)
Size A3	Document Number M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	25 of 71



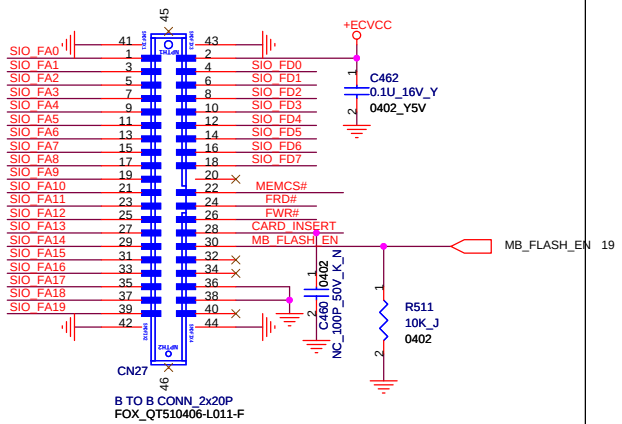
XBUS BIOS ROM

DVT : delete winbond

WINBOND



JIG-120 DEBUG PORT



EXTERNAL XBUS ROM INTERFACE

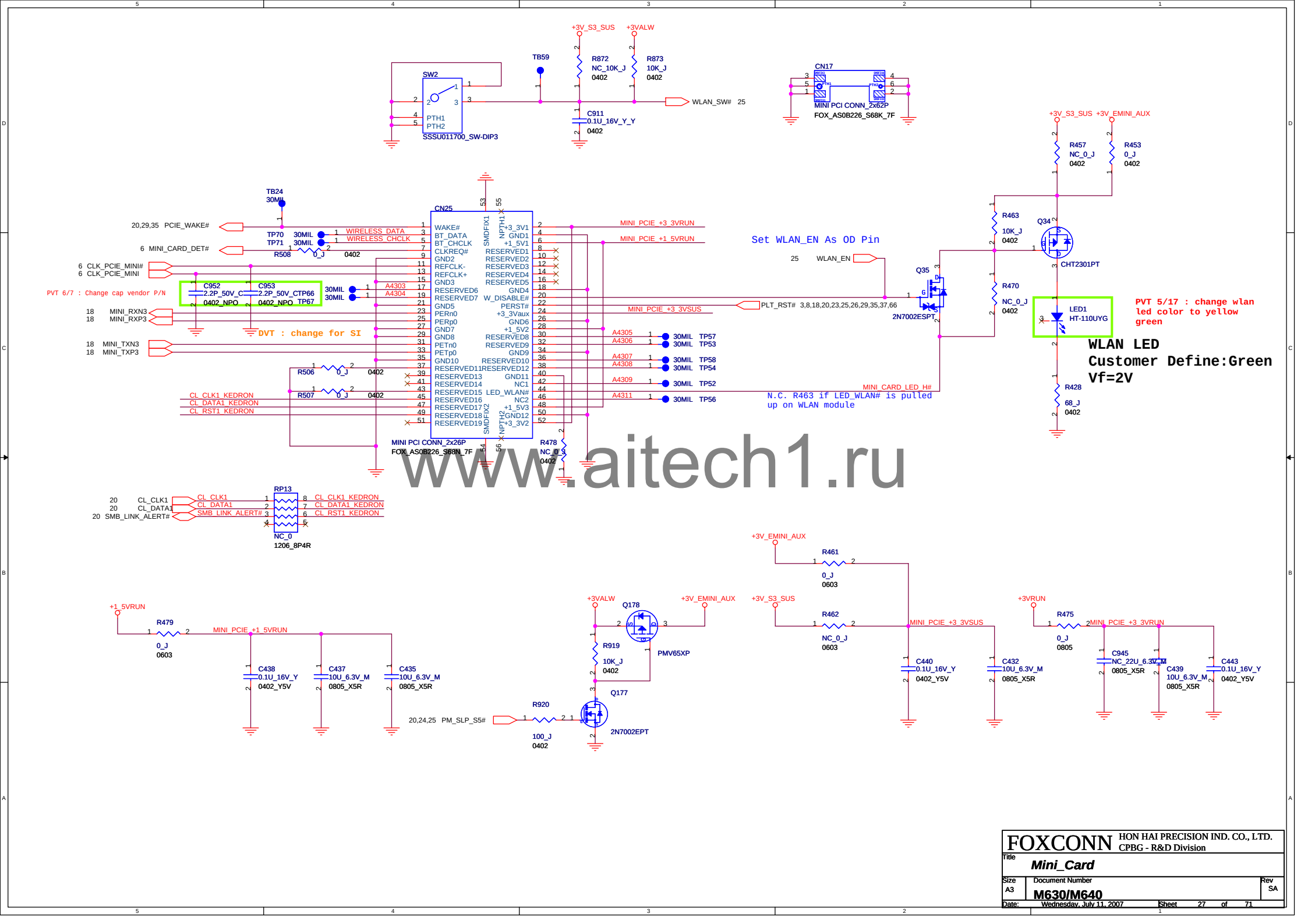
DVT : delete winbond

JTAG INTERFACE

WINBOND

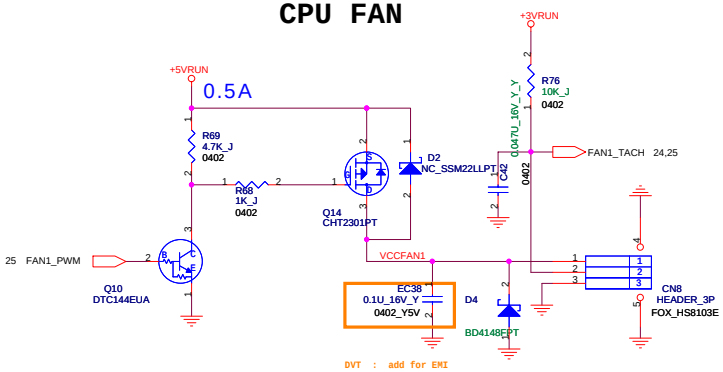
EXTERNAL SPI ROM INTERFACE

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Flash ROM/X-Bus CONN*		
Size: A3	Document Number: M630/M640	Rev: SA
Date: Wednesday, July 11, 2007	Sheet 26 of 71	

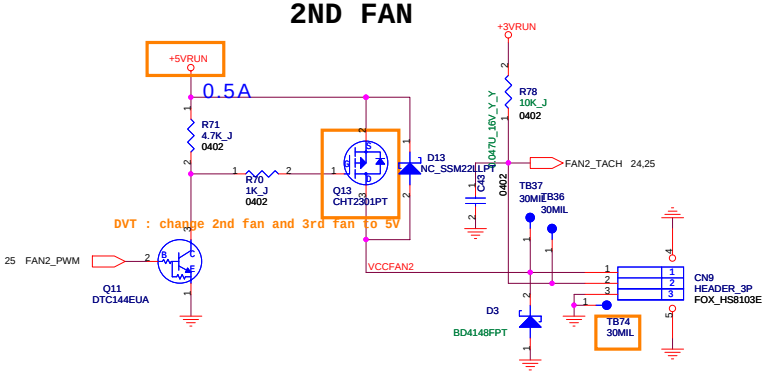


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*Mini_Card*
Size A3	Document Number **M630/M640**
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	27 of 71

CPU FAN

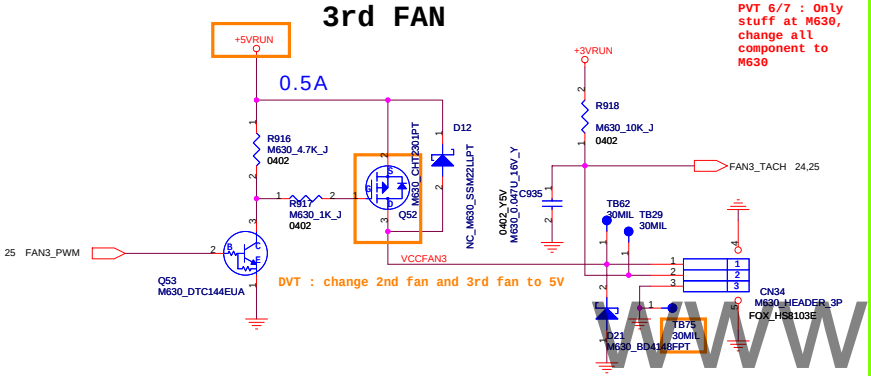


2ND FAN

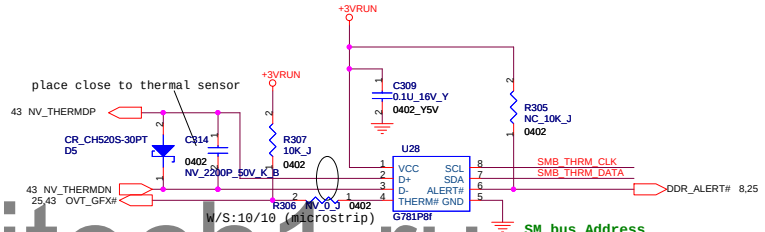


3rd FAN

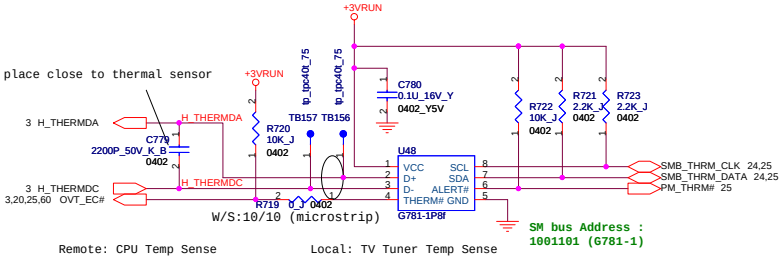
PVT 6/7 : Only stuff at M630, change all component to M630



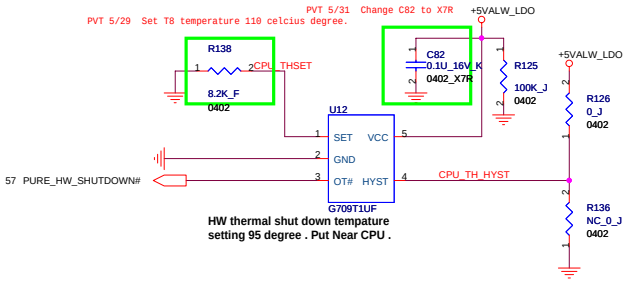
VGA SENSOR



CPU SENSOR



HW THERMAL PROTECTION

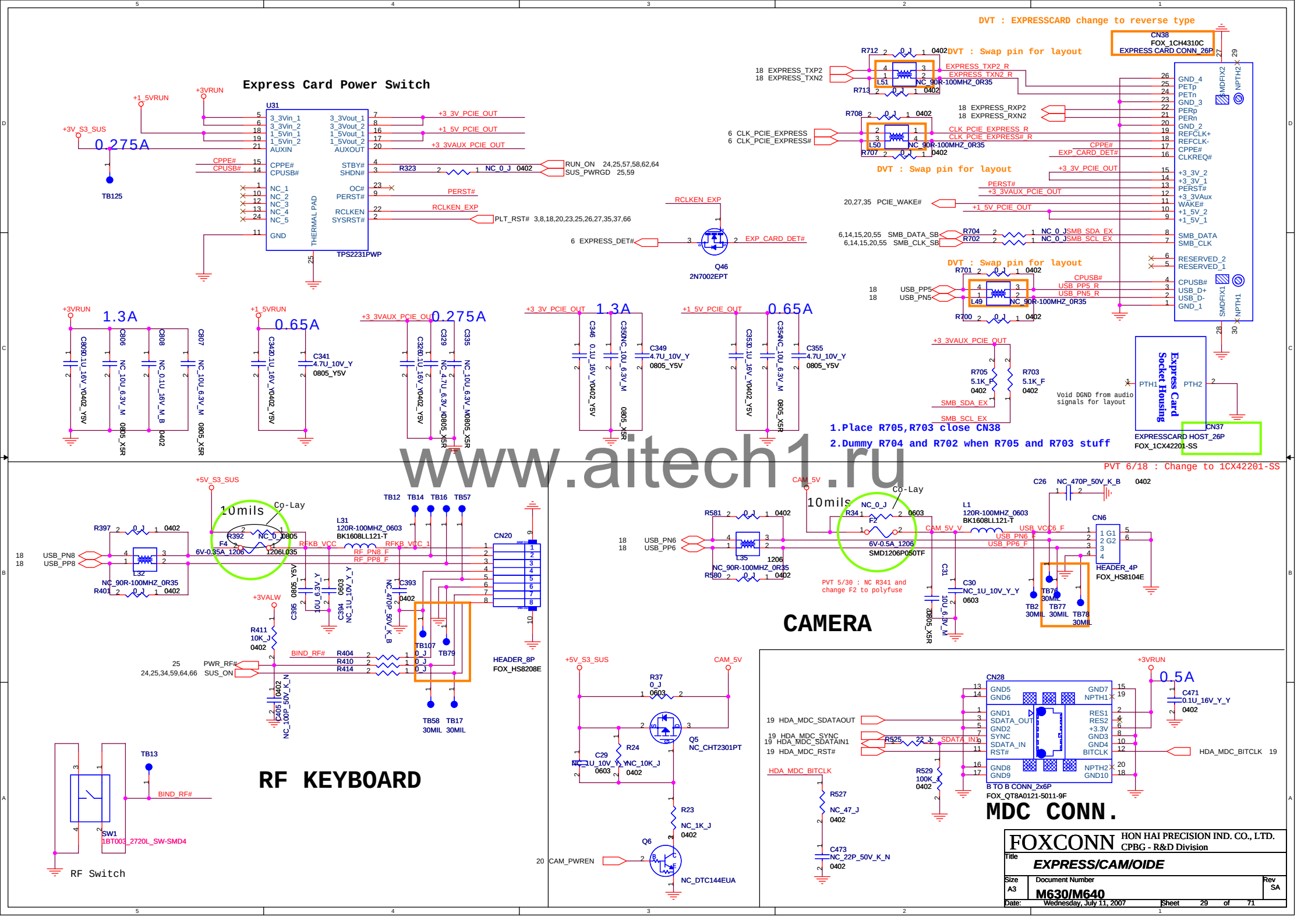


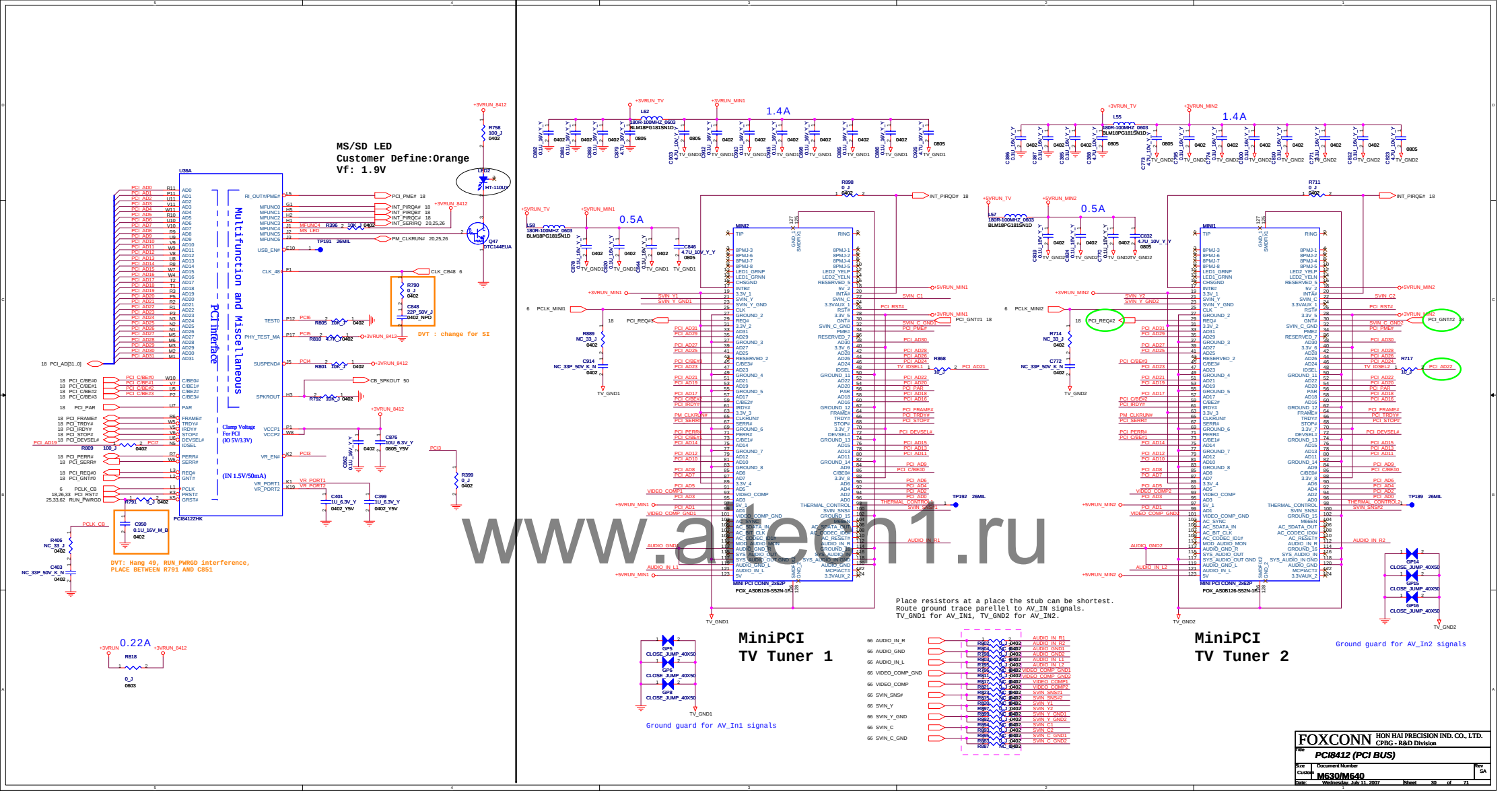
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

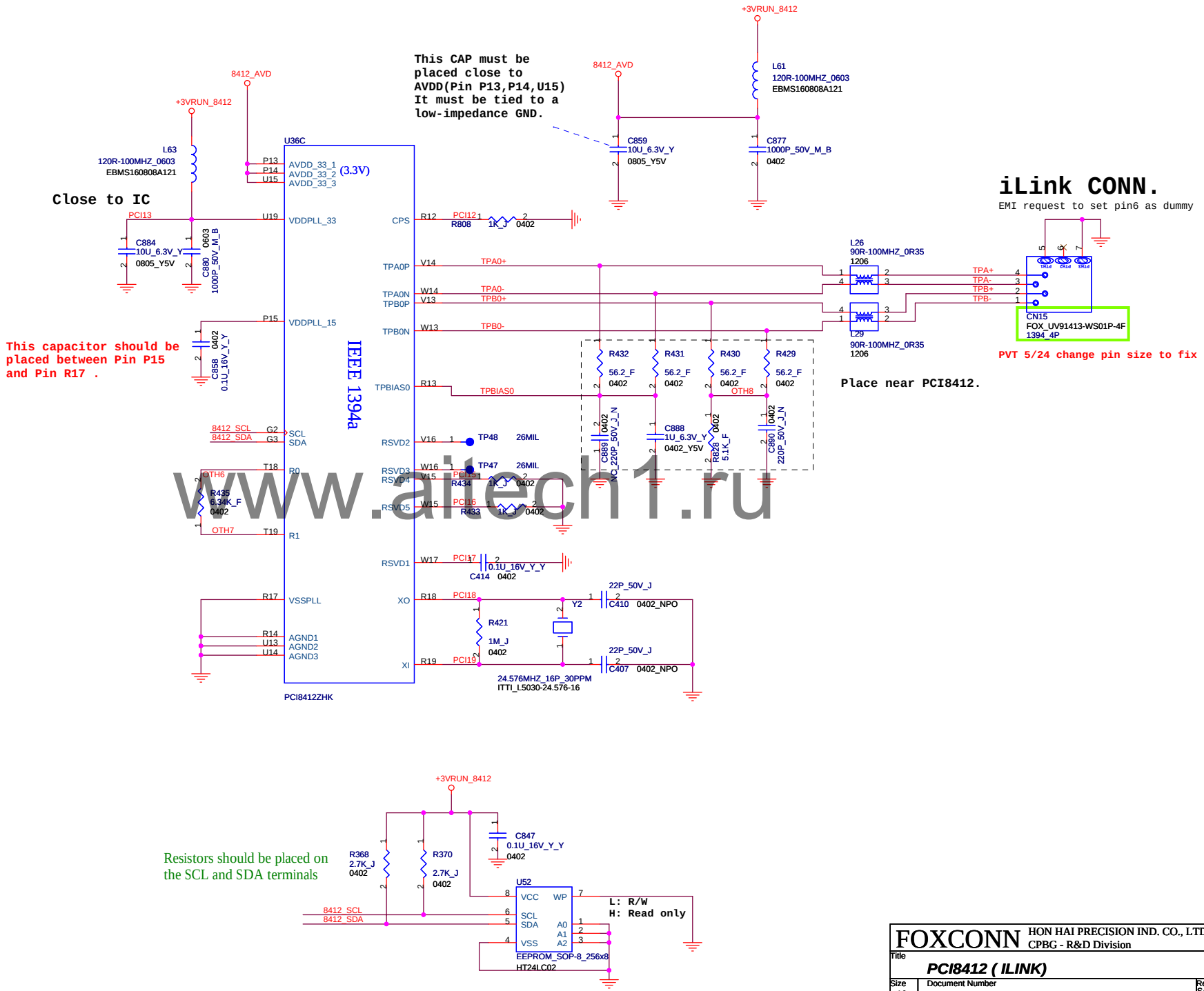
Title: FAN/HW THERMAL PROTECT

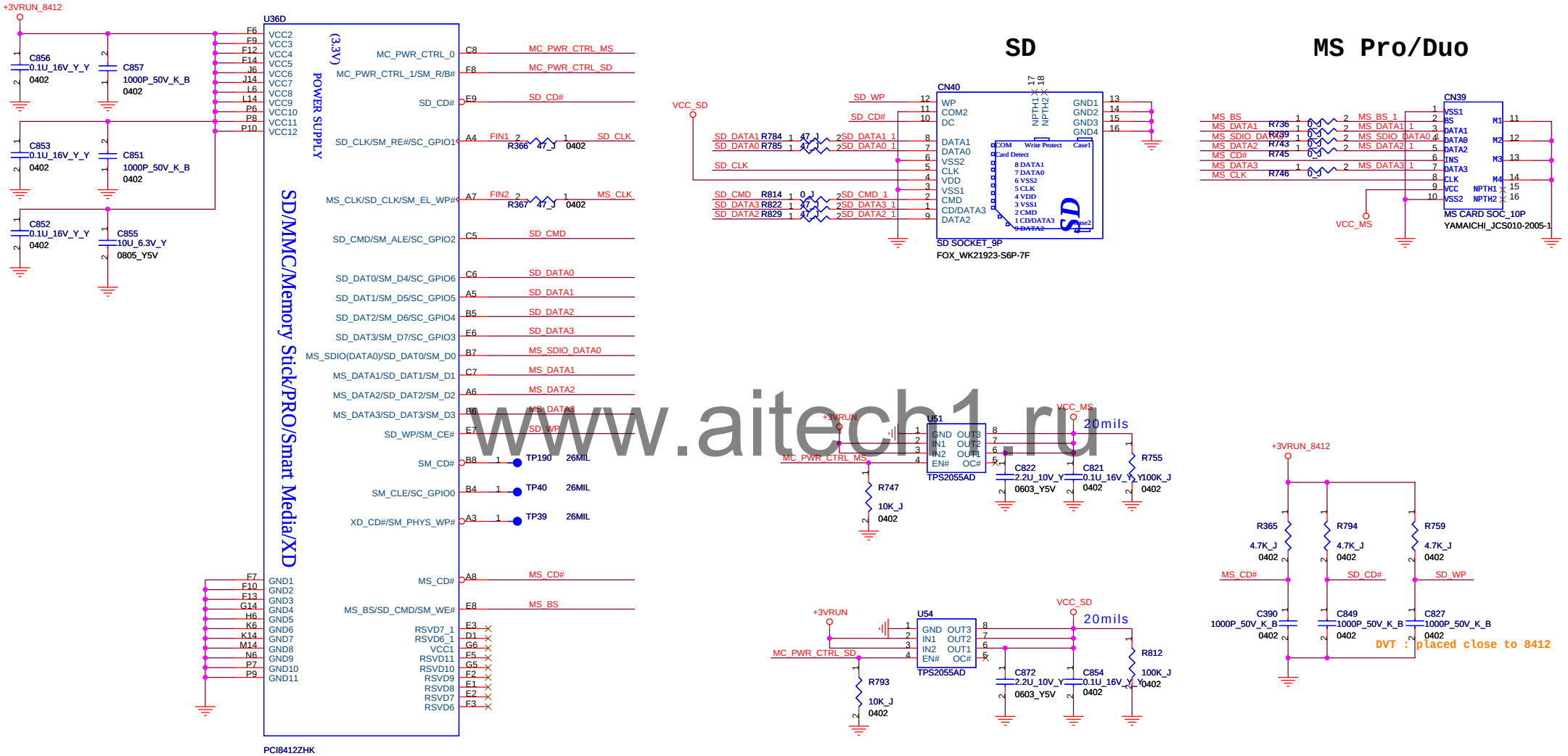
Size: Custom | Document Number: M630/M640 | Rev: SA

Date: Friday, July 27, 2007 | Sheet 28 of 71




MS/SD LED
Customer Define:Orange
Vf: 1.9V
Multifunction and Miscellaneous
PCI Interface
PCI8412ZHK
Clamp Voltage For PCI (IO 3V/3.3V)
(IN 1.5V/50mA)
DVT: Hang 49, RUN_PWRGD interference, PLACE BETWEEN R791 AND C851
DVT : change for SI
0.22A
1.4A
0.5A
MiniPCI TV Tuner 1
MiniPCI TV Tuner 2
Ground guard for AV_In1 signals
Ground guard for AV_In2 signals
Place resistors at a place the stub can be shortest.
Route ground trace parellel to AV_IN signals.
TV_GND1 for AV_IN1, TV_GND2 for AV_IN2.
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
PCI8412 (PCI BUS)
M630/M640
Wednesday, July 11, 2007
Sheet 30 of 71





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI8412 (MS/SD)/MDC
Size A3	Document Number M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
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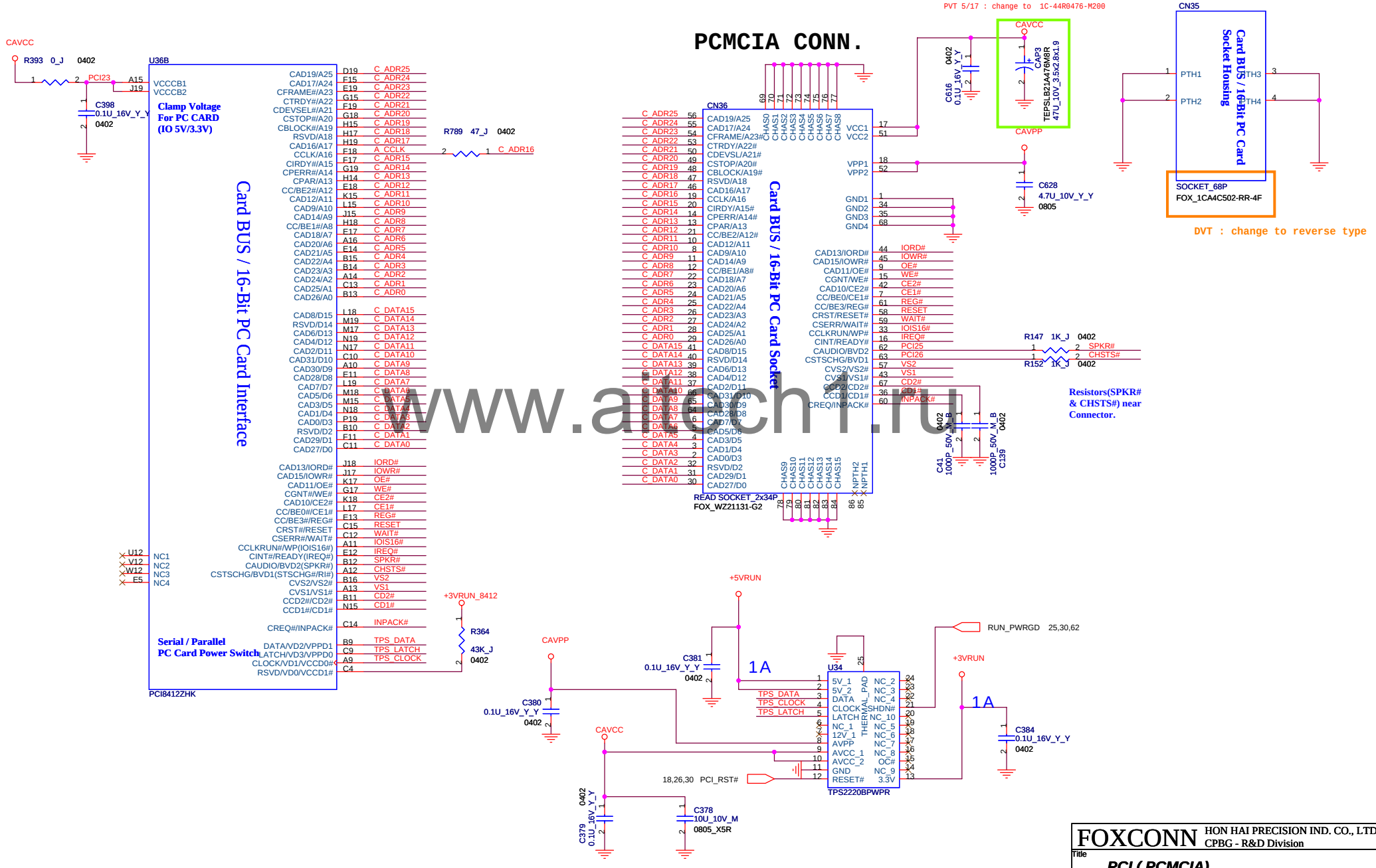
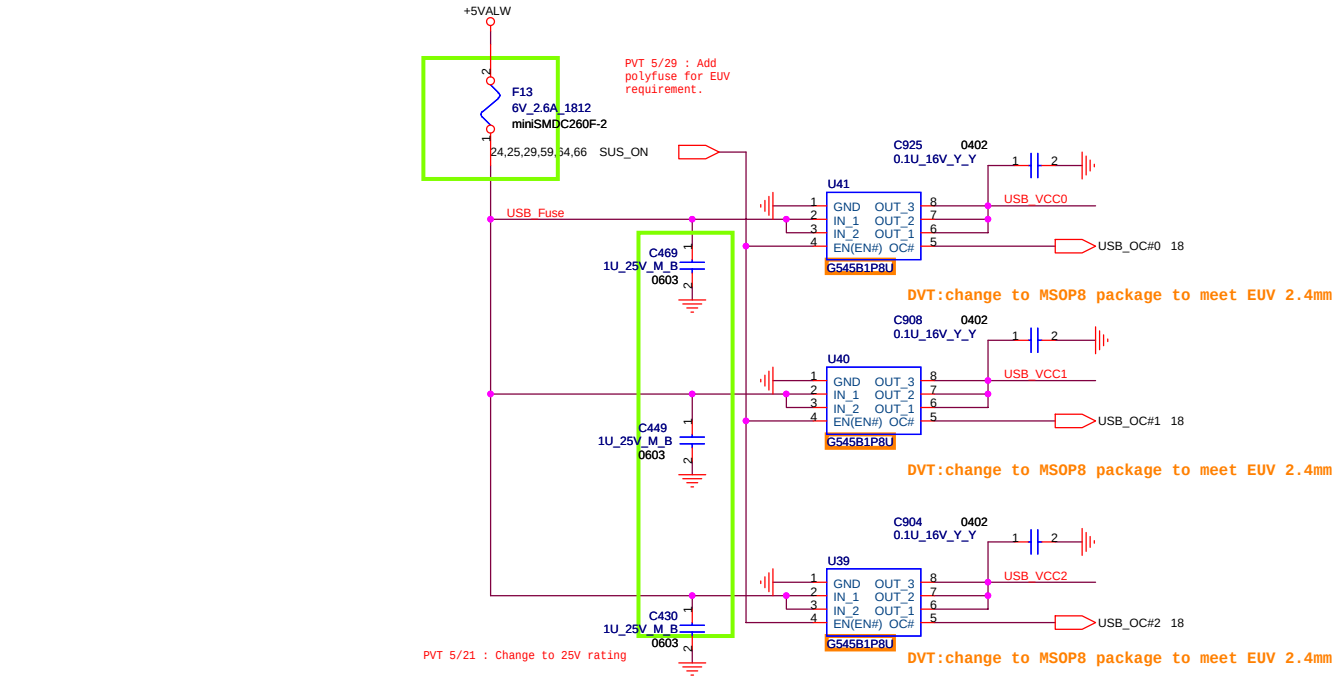
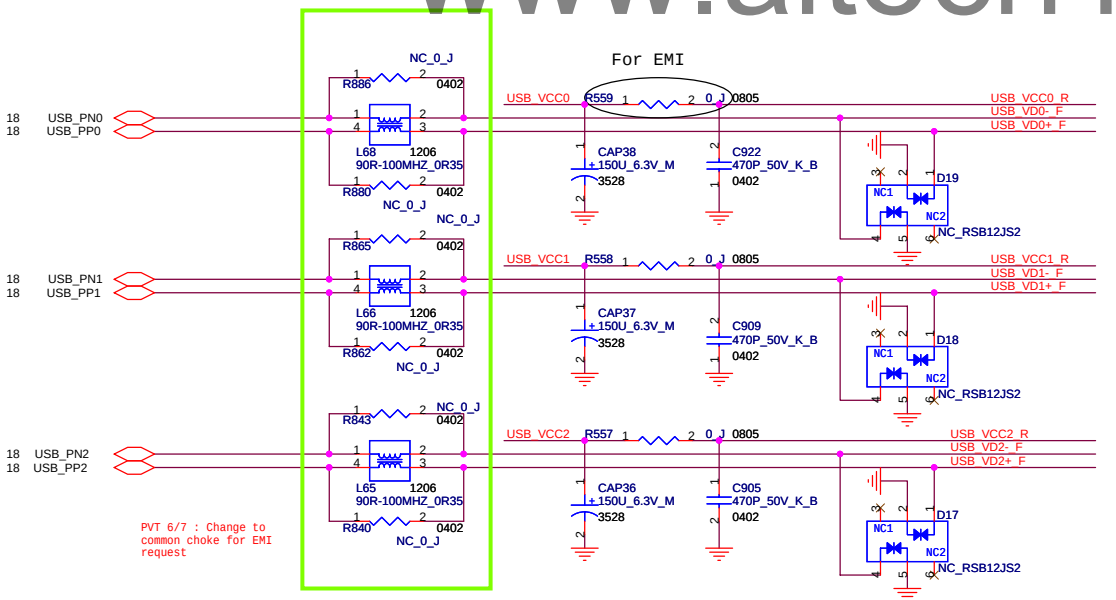
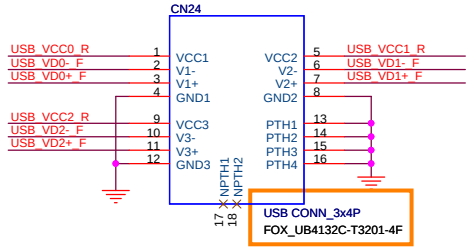


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (PCMCIA)
Size A3	Document Number
Rev SA	
Date: Wednesday, July 11, 2007	Sheet 33 of 71





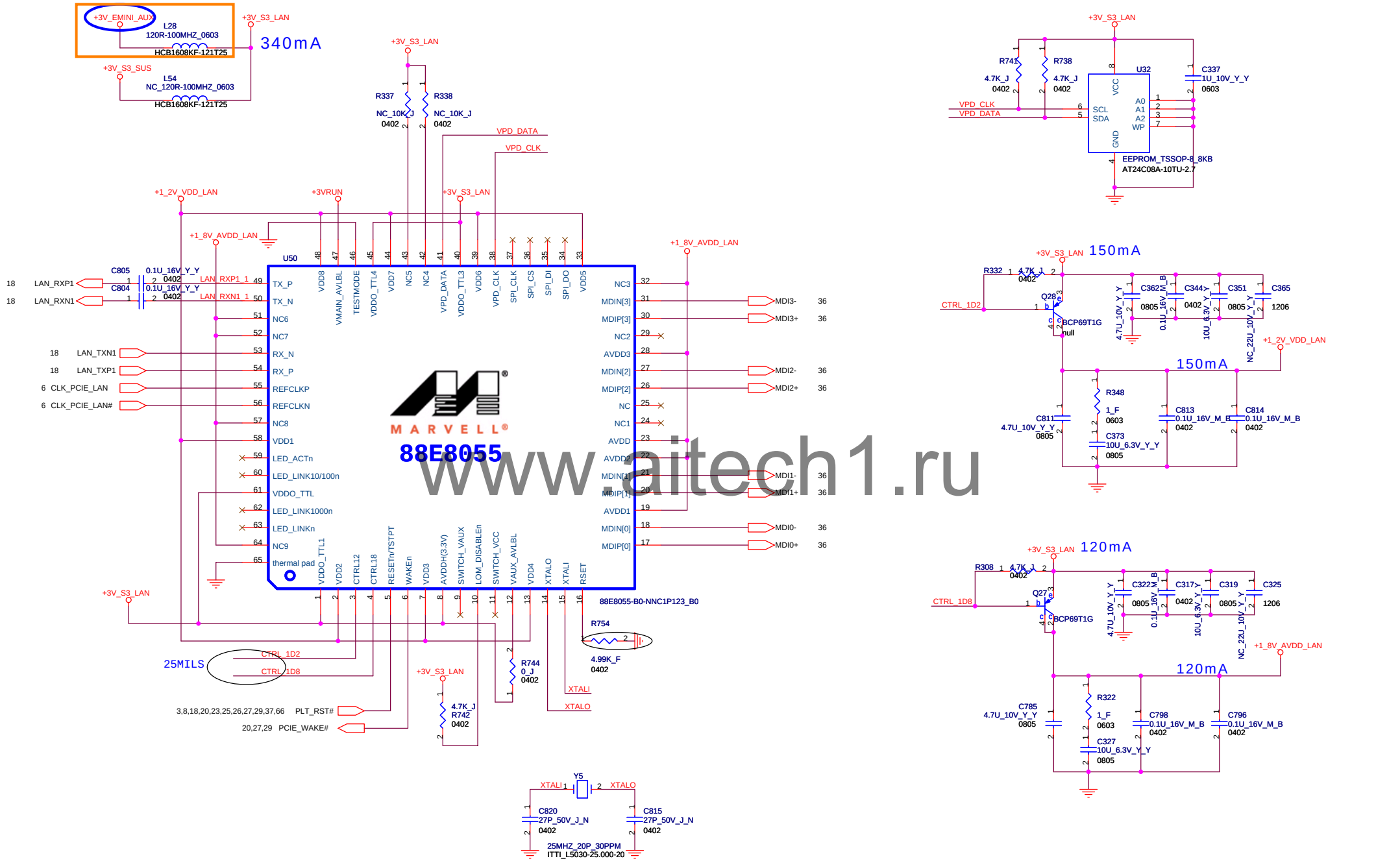
REAR USB CONN X 3



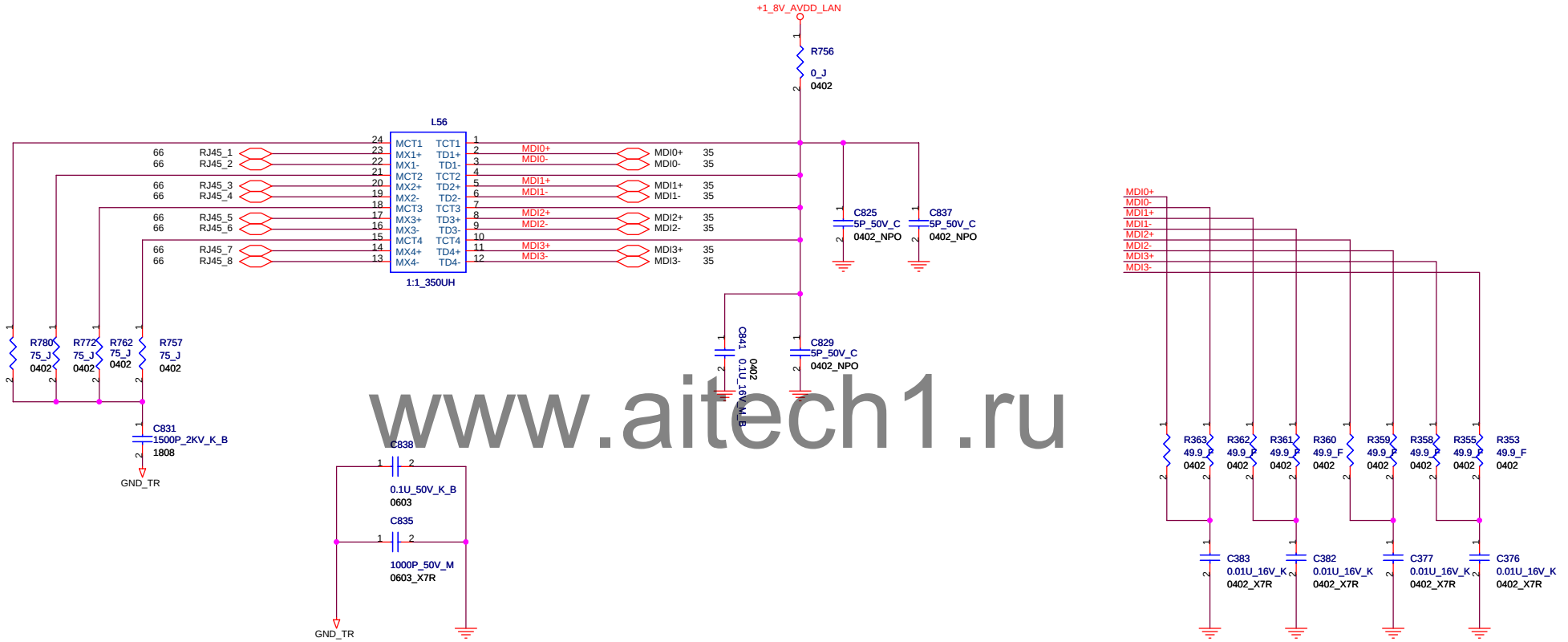
DVT change to black color

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: USB2.0 PORT		
Size: A3	Document Number: M630/M640	Rev: SA
Date: Wednesday, July 11, 2007	Sheet 34 of 71	

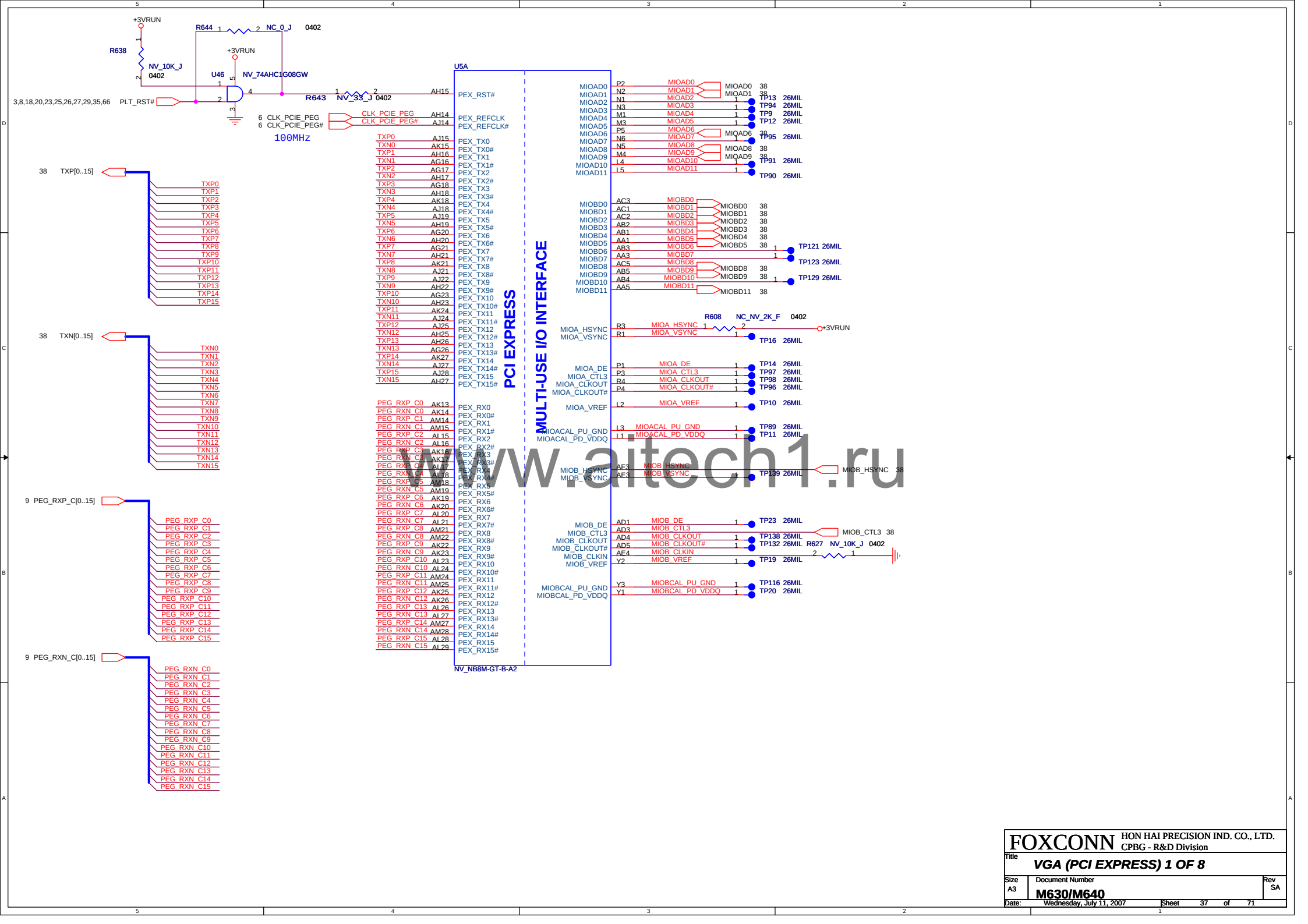
To support S4 wake up DVT : support S4 wake up , power change to +3V_EMINI_AUX



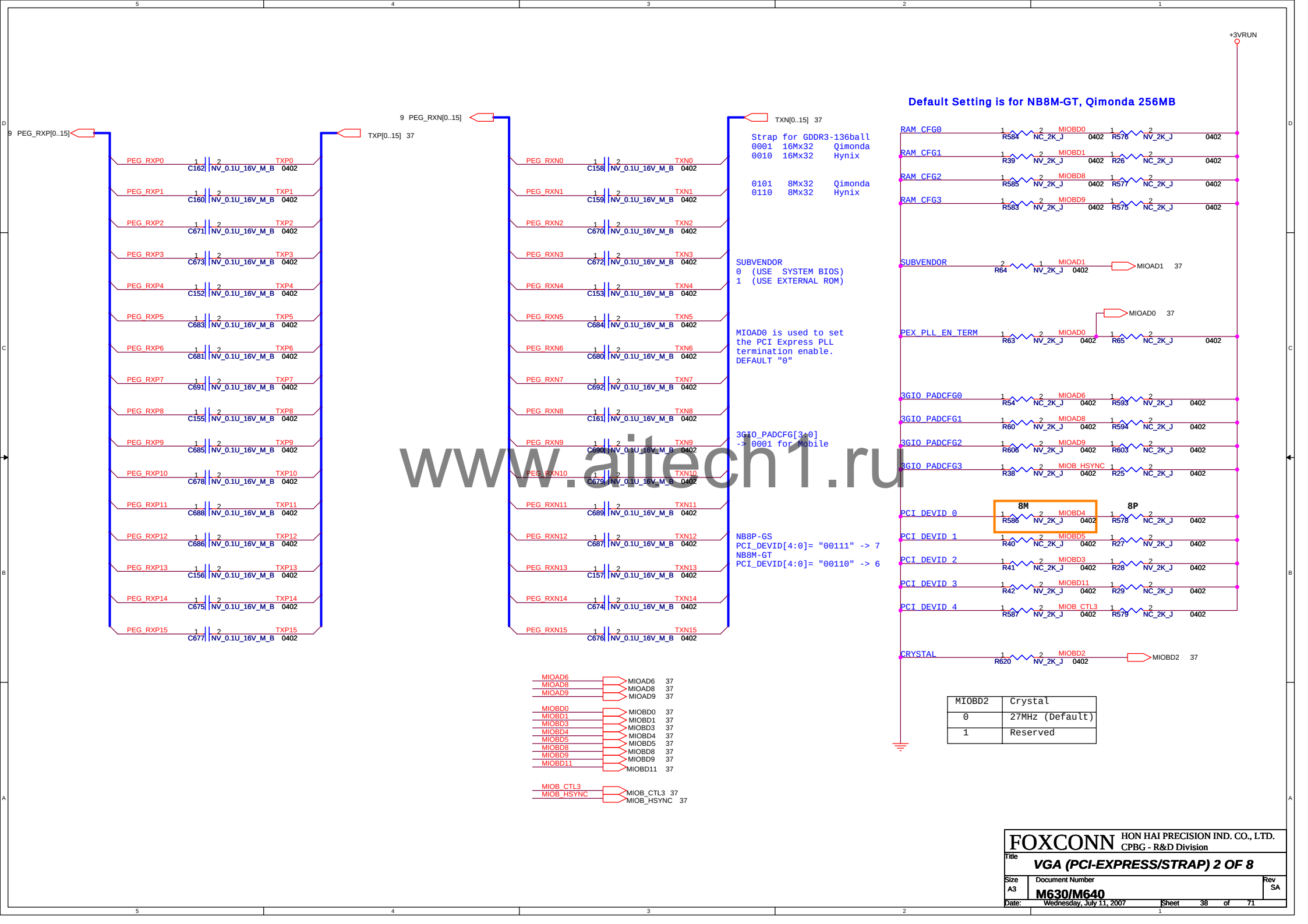
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	LAN Controller
Size	A3
Document Number	M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	35 of 71

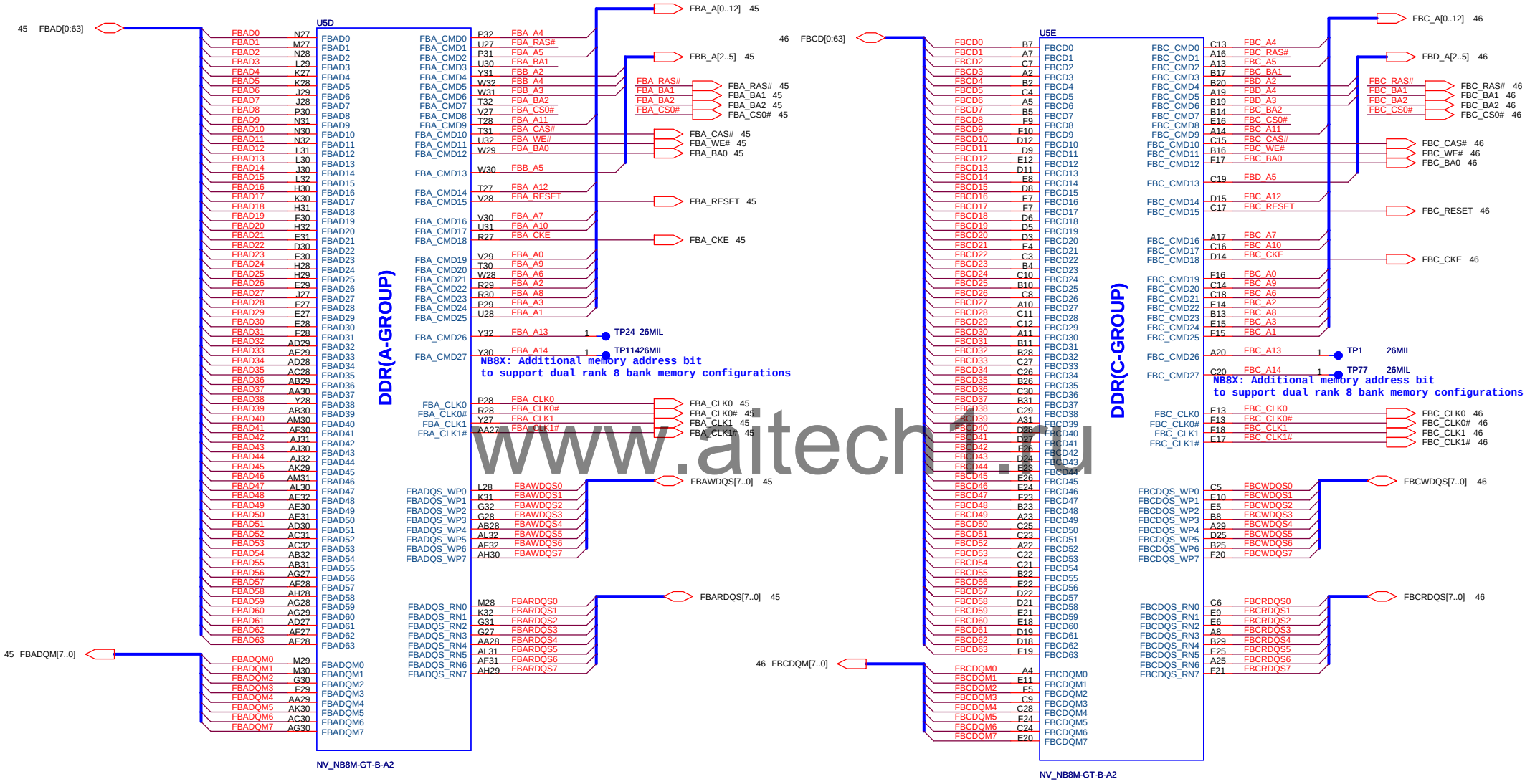


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN Transformer	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 36 of 71	

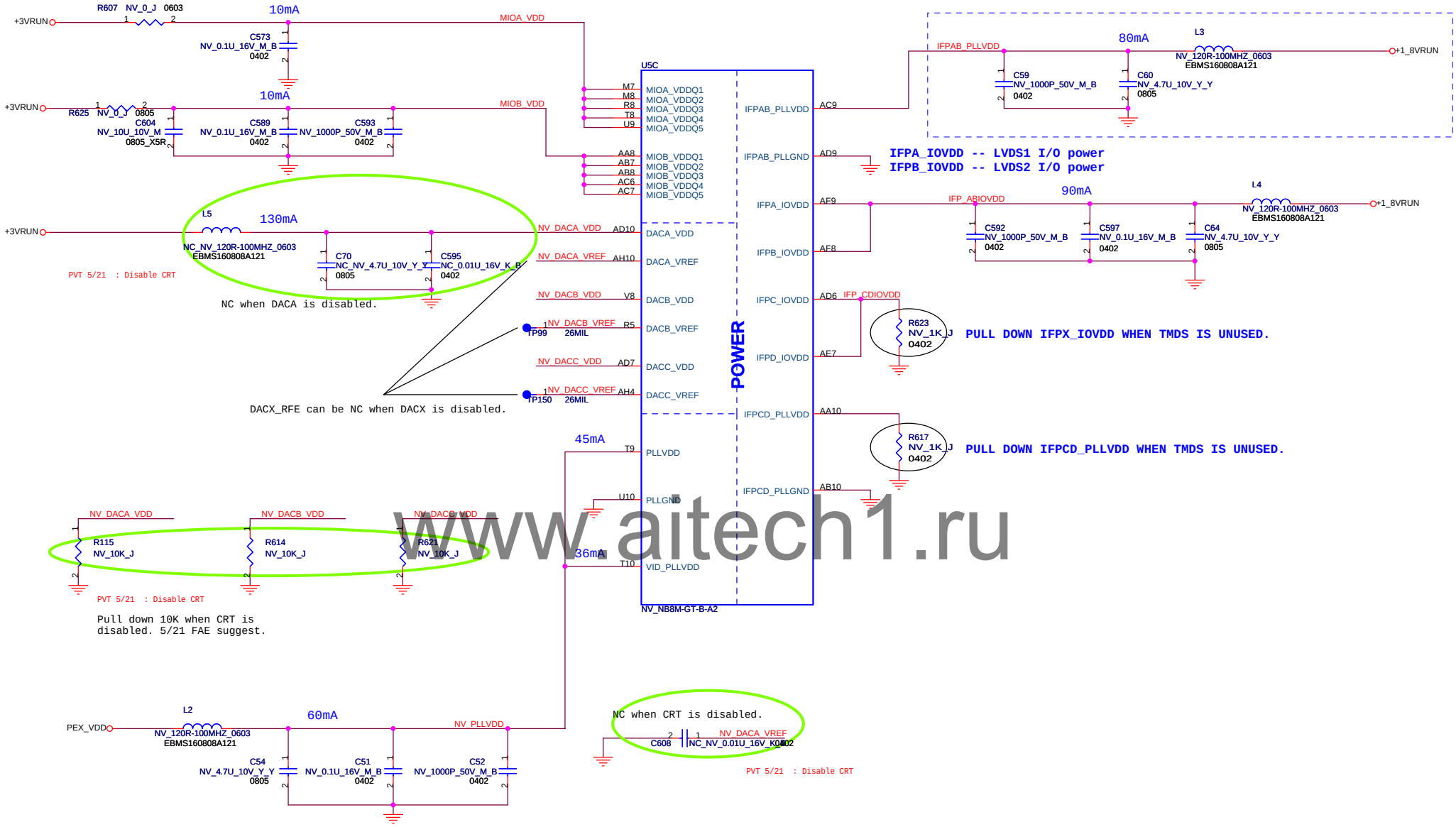


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (PCI EXPRESS) 1 OF 8
Size A3	Document Number M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	37 of 71

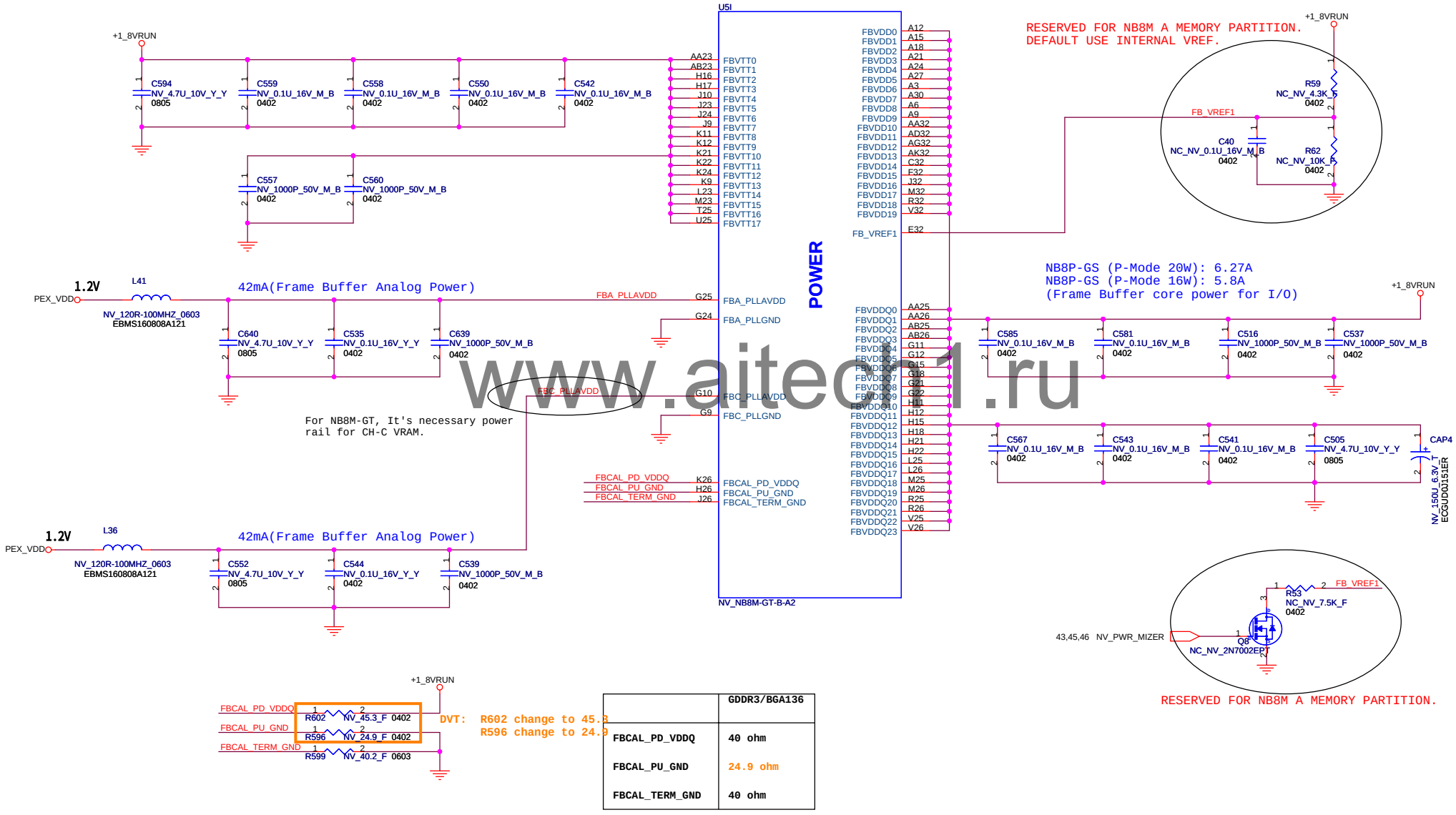




FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (GDDR) 3 OF 8
Size A3	Document Number M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	39 of 71



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (POWER) 4 OF 8
Size A3	Document Number M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	40 of 71



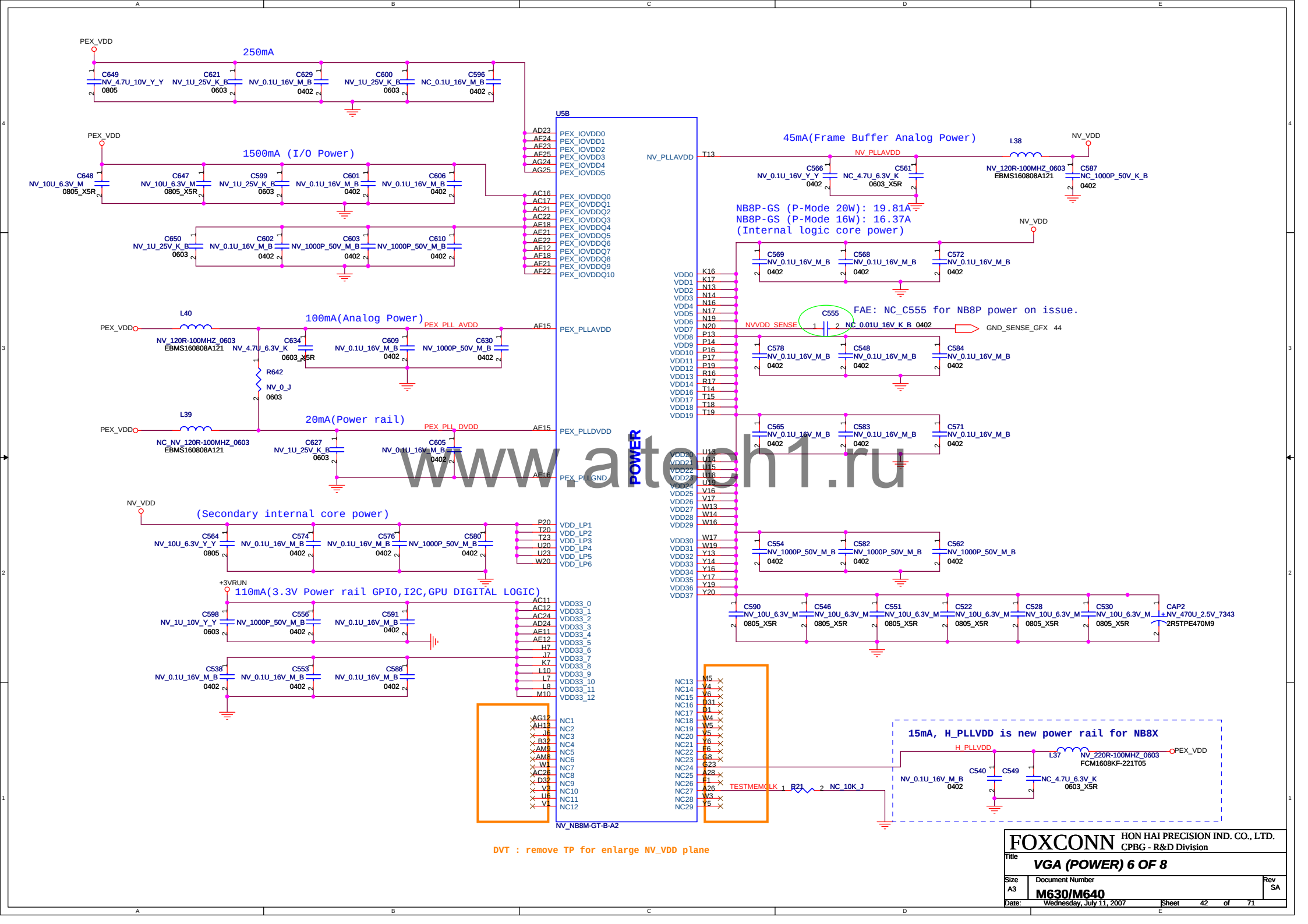
	GDDR3/BGA136
FBCAL_PD_VDDQ	40 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40 ohm

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (POWER) 5 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 41 of 71



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (POWER) 6 OF 8
Size	A3
Document Number	M630/M640
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	42 of 71

NB8X: Slave I2C/SMBUS
compatible interface. (Addr: 0x9e)

2006/8/30 Update

GPIO TABLE			
	I/O	Inter pull low	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)
GPIO1	I	Yes	DVI Hot Plug Detect 1(HPD1)
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM) **Active High**
GPIO3	O	No	Panel Power(LCD0_VDD) **Active Low**
GPIO4	O	Yes	LCDBacklight enable(LCD0_BL_EN) **Active High**
GPIO5	O	Yes	GPU Voltage selection (GPU_VID0)
GPIO6	O	Yes	GPU Voltage selection (GPU_VID1)
GPIO7	O	Yes	GPU/Memory Voltage selection(GPU_VID2/MEM_VID)
GPIO8	I/OD	No	Over Temperature Shutdown **Active Low**
GPIO9	I/OD	No	THERMAL ALERT I/O, FAN PWM Control **Active Low**
GPIO10	I/O	No	Memory Vref switch(MEM_VREF)
GPIO11	O	No	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	I	No	AC power detect input (AC_DET)
GPIO13	O	No	Power supply control (PWR_CTRL0)
GPIO14	O	No	Power supply control (PWR_CTRL1)

Could be NC if HDCP is not used.

Boundary scans in conjunction with testmode pin.

DVT : remove TP for enlarge NV_VDD plane

DVT : remove TP for enlarge NV_VDD plane

DVT : remove TP for enlarge NV_VDD plane

DVT : GPIO5 connect to VGA power

DVT : value change to NV_*

NB8X: XTALIN use 3.3V level

OVERTEMP LATCHING CIRCUIT

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

0 = connect to GND
M= unconnected
1 = connect directly to VDD

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

nVidia support Down -1.25%

This chip can use MK1726 or P1819B

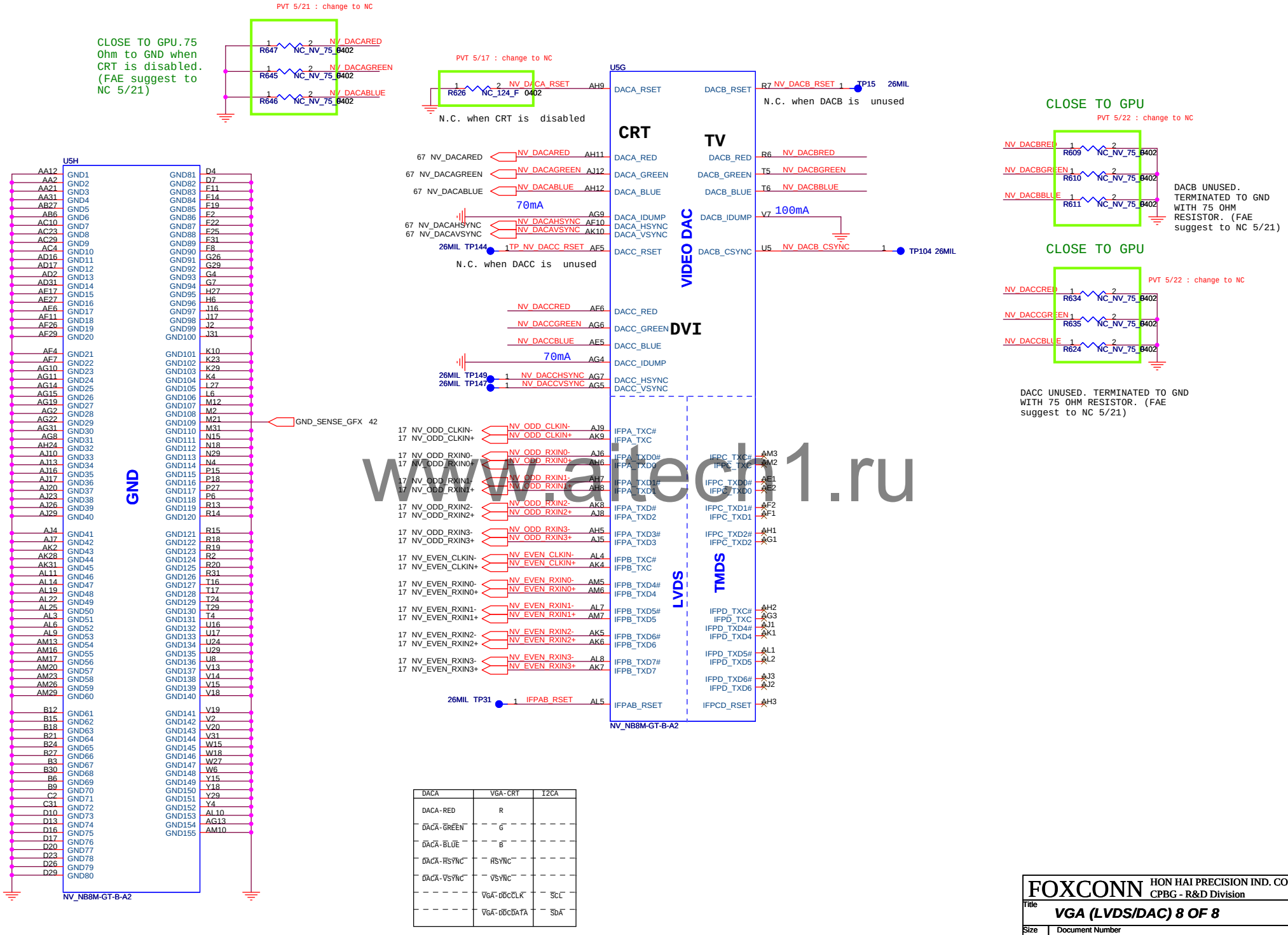
R616 place near GPU
R79 place near spectrum chip

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (MULTIUSE) 7 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 43 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (LVDS/DAC) 8 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Friday, July 27, 2007 | Sheet 44 of 71

PVT 6/5 Reserve for WL Noise

+1_8VRUN

U4

U9

U3037_RFU 1

U3036_RFU 1

TP3 26MIL

TP21 26MIL

U3037_ZQ A4

U3036_ZQ A4

NV_SDRAM_PG-TFBGA-136_512MB
HYB18H512321BF-14

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

FBAD[0:63] 39
FBADQM[7..0] 39
FBARDQS[7..0] 39
FBAWDQS[7..0] 39

R66,R85 (120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

PVT 5/24 remove R52, C39 (FAE suggestion)

PVT 5/24 remove R93, C63 (FAE suggestion)

PVT : FAE suggest to 2200 pF

NV_PWR_MIZER H 40%
L 70%

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Title: VRAM (GDDR3) 1 OF 4

Size A3 | Document Number: M630/M640 | Rev SA

Date: Wednesday, July 11, 2007 | Sheet 45 of 71

PVT 6/5 Reserve for WL Noise

PVT 6/5 Reserve for WL Noise

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

R6,R15(120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

PVT 5/24 remove R17, C24 (FAE suggestion)

PVT 5/24 remove R561, C487 (FAE suggestion)

PVT : FAE suggest to 2200 pF

PVT : FAE suggest to 2200 pF

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Title: VRAM (GDDR3) 2 OF 4

Size: A3 | Document Number: M630/M640 | Rev: SA

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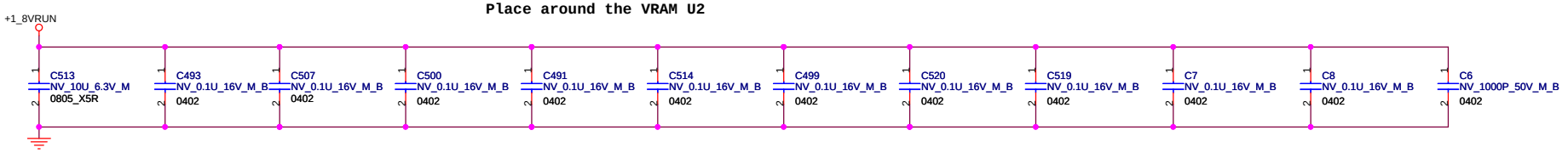
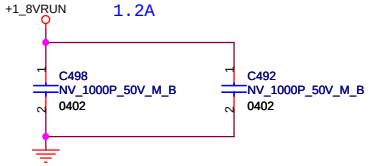
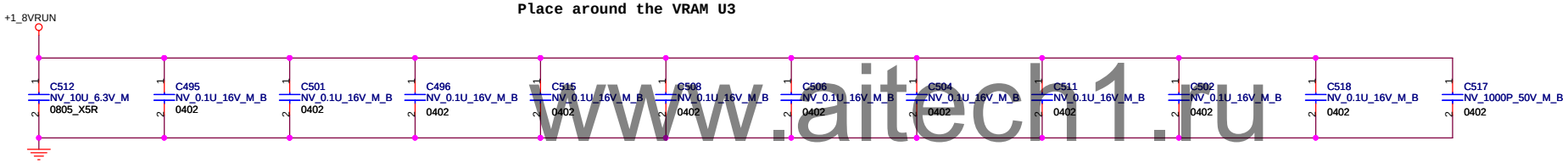
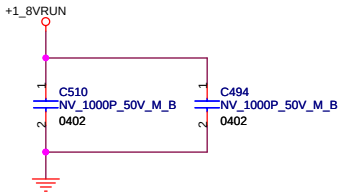
Place around the VRAM U2





Place around the VRAM U3





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: VRAM (GDDR3) 2 OF 4		
Size: A3	Document Number: M630/M640	Rev: SA
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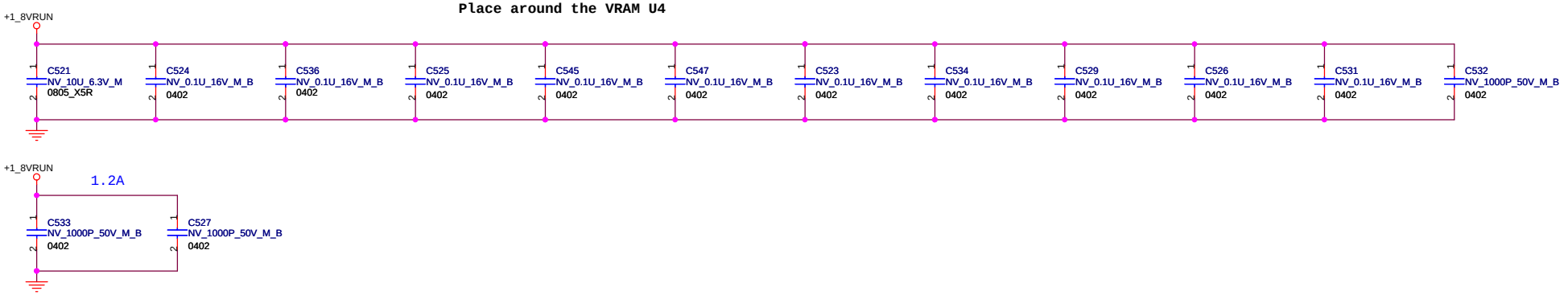
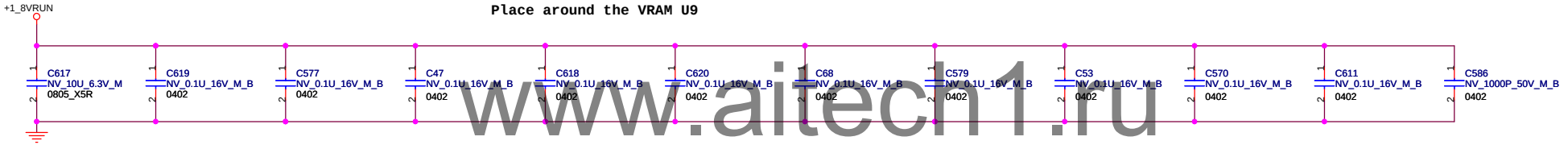
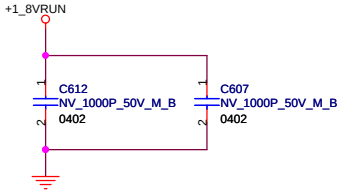
Place around the VRAM U4



Place around the VRAM U9





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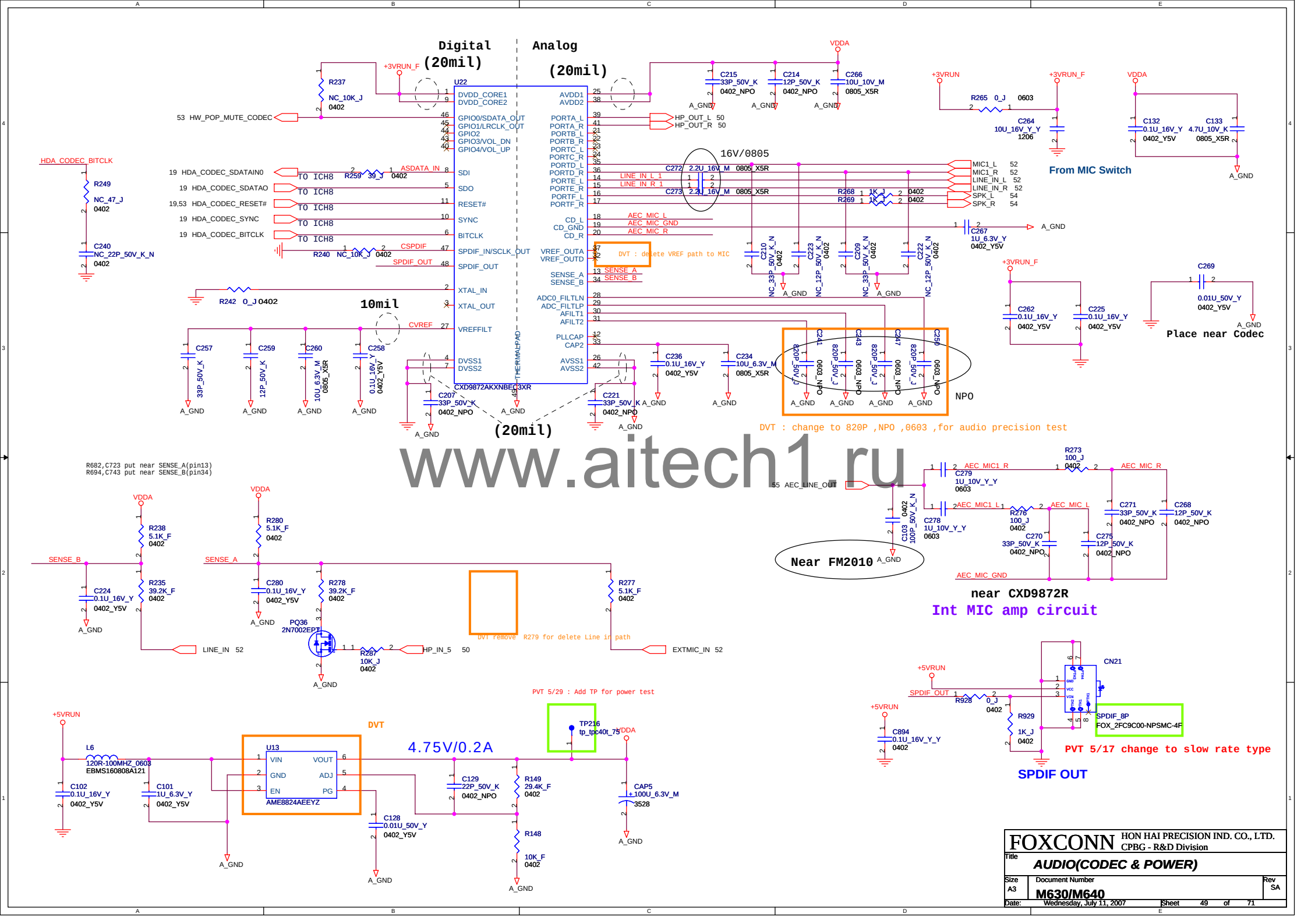
Title: *VRAM (POWERBYPASS) 4 OF 4*

Size: A3 | Document Number: **M630/M640** | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 48 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
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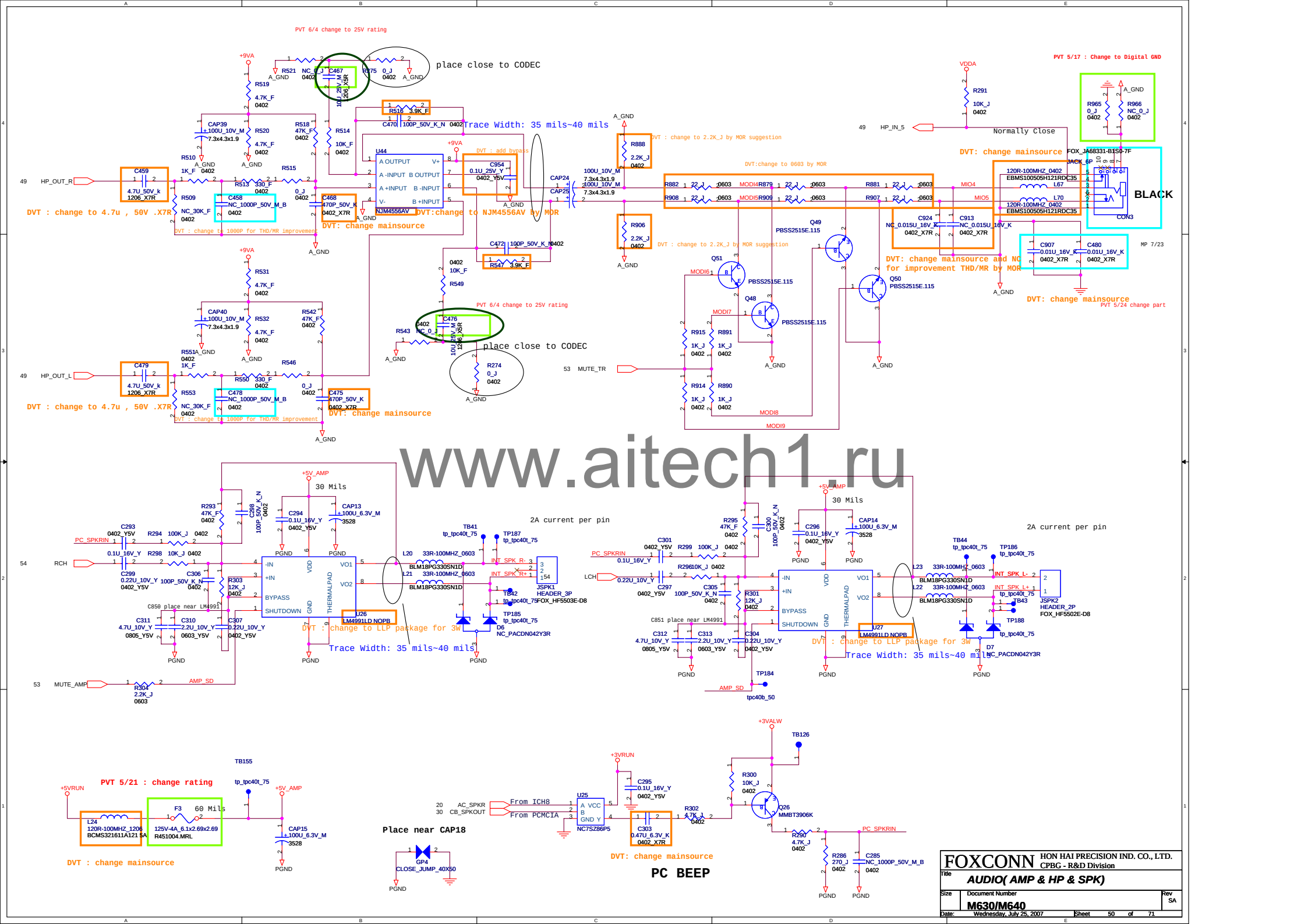
Title: AUDIO(CODEC & POWER)

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 49 of 71


PVT 6/4 change to 25V rating
place close to CODEC
Trace Width: 35 mils~40 mils
DVT : add bypass
DVT:change to NJM4556AV by MOR
DVT : change to 4.7u , 50V .X7R
DVT: change mainsource
DVT : change to 1000P for THD/MR improvement
PVT 6/4 change to 25V rating
place close to CODEC
DVT : change to 4.7u , 50V .X7R
DVT: change mainsource
DVT : change to 1000P for THD/MR improvement
PVT 5/17 : Change to Digital GND
Normally Close
DVT: change mainsource
DVT : change to 2.2K_J by MOR suggestion
DVT:change to 0603 by MOR
DVT : change to 2.2K_J by MOR suggestion
DVT: change mainsource and NC for improvement THD/MR by MOR
DVT: change mainsource
PVT 5/24 change part
BLACK
30 Mils
2A current per pin
DVT : change to LLP package for 3W
Trace Width: 35 mils~40 mils
30 Mils
2A current per pin
DVT : change to LLP package for 3W
Trace Width: 35 mils~40 mils
PVT 5/21 : change rating
DVT : change mainsource
Place near CAP18
DVT: change mainsource
PC BEEP
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CPBG - R&D Division
AUDIO(AMP & HP & SPK)
M630/M640
Wednesday, July 25, 2007
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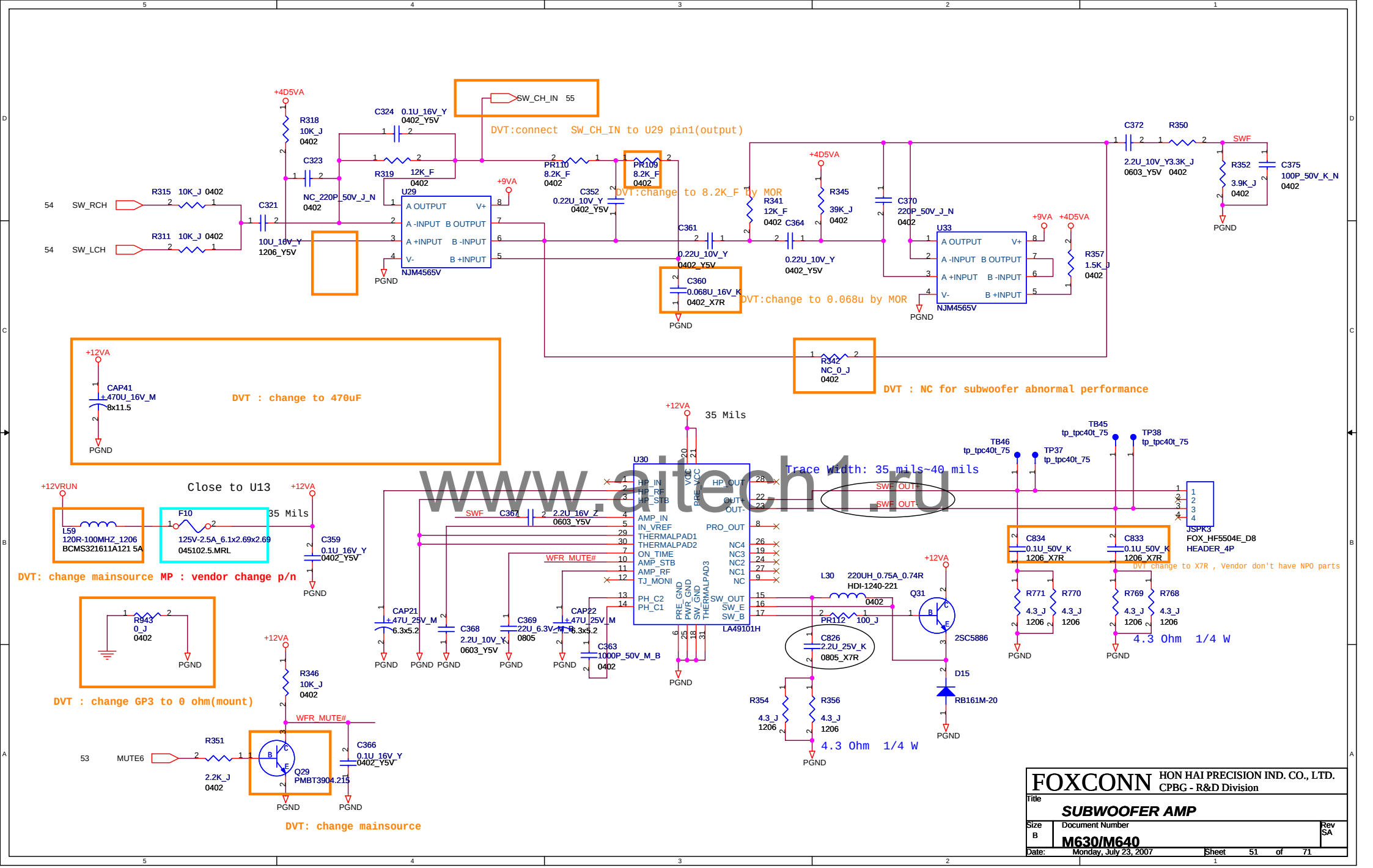

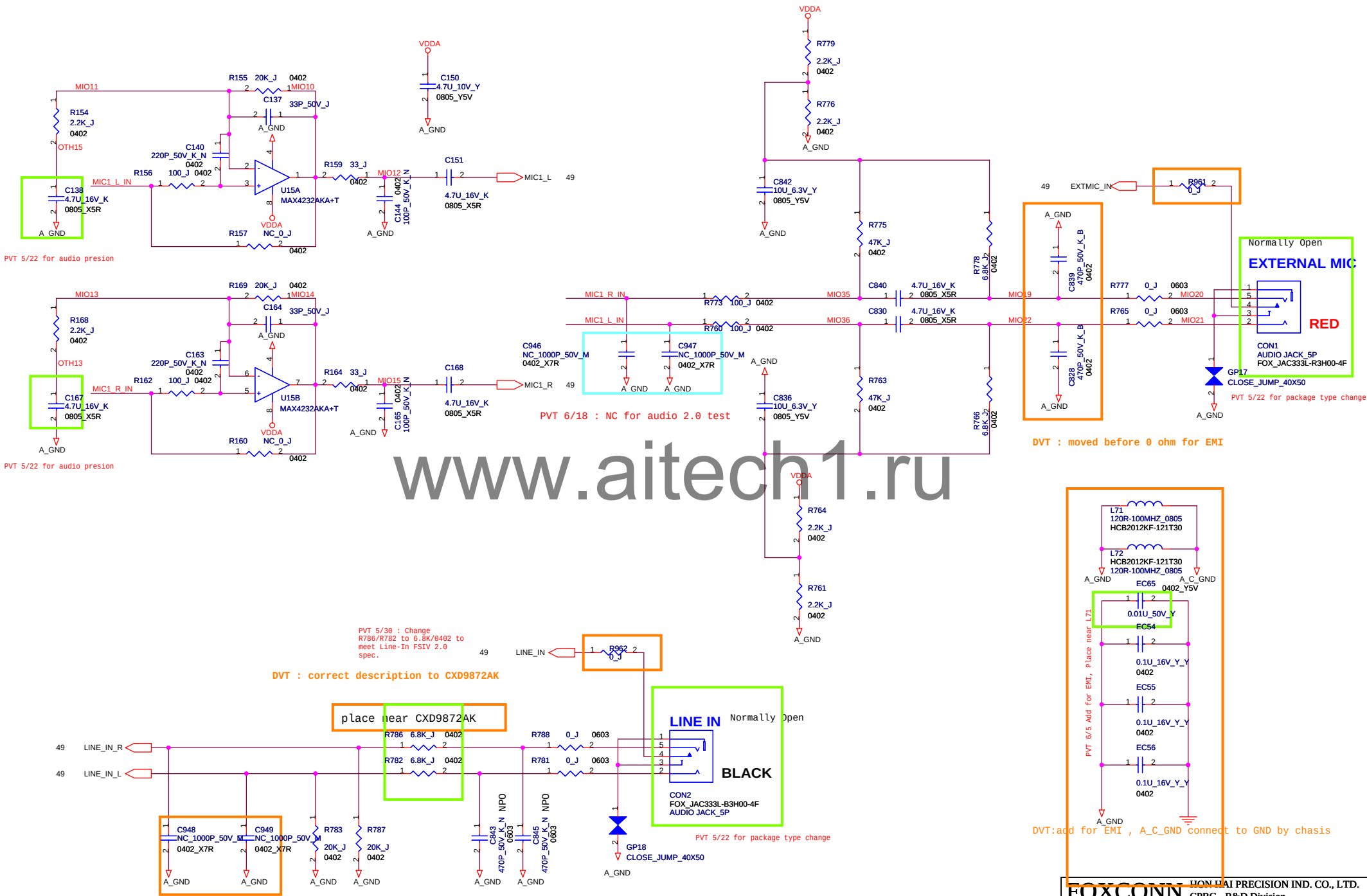

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: AUDIO(EXT MIC & LINE IN & SPDIF)

Size	Document Number	Rev
A3	M630/M640	SA

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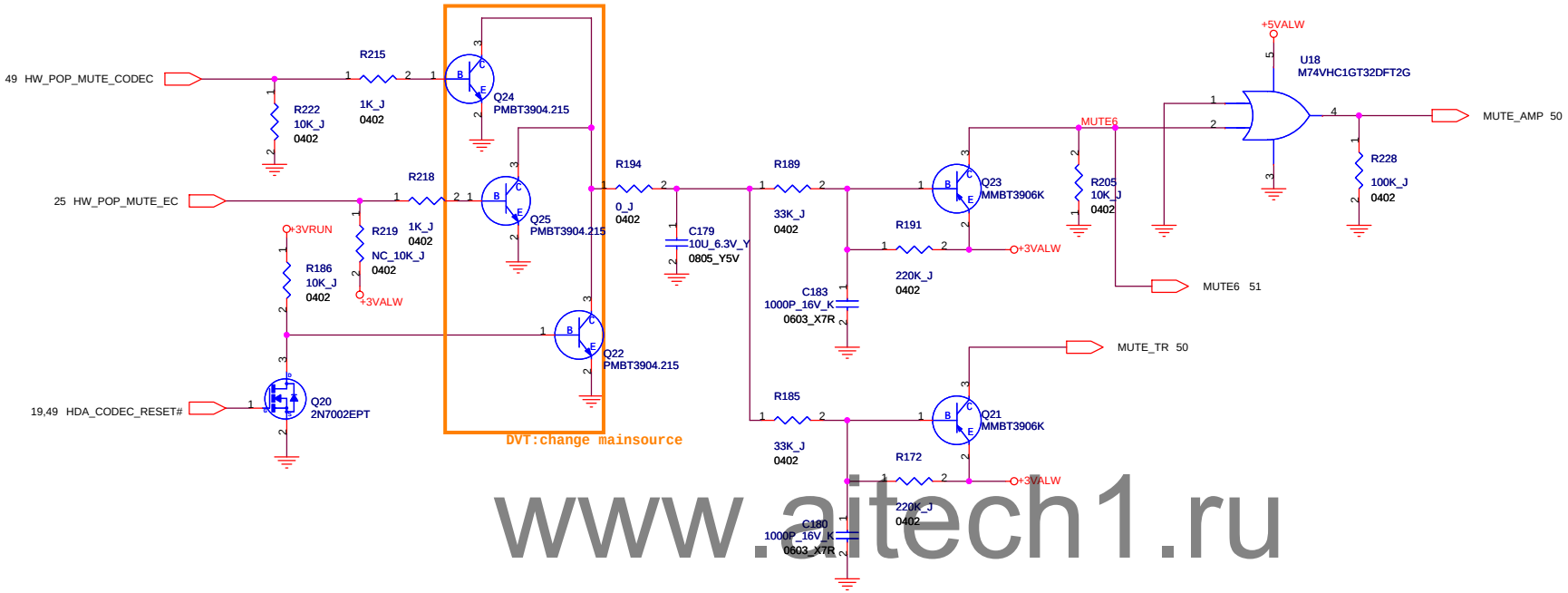
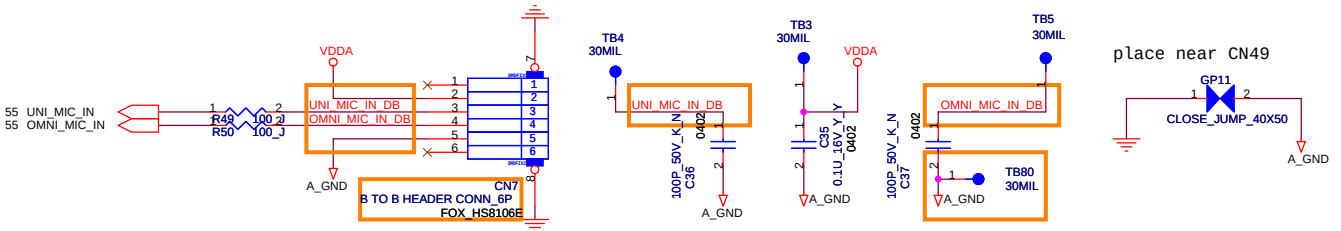
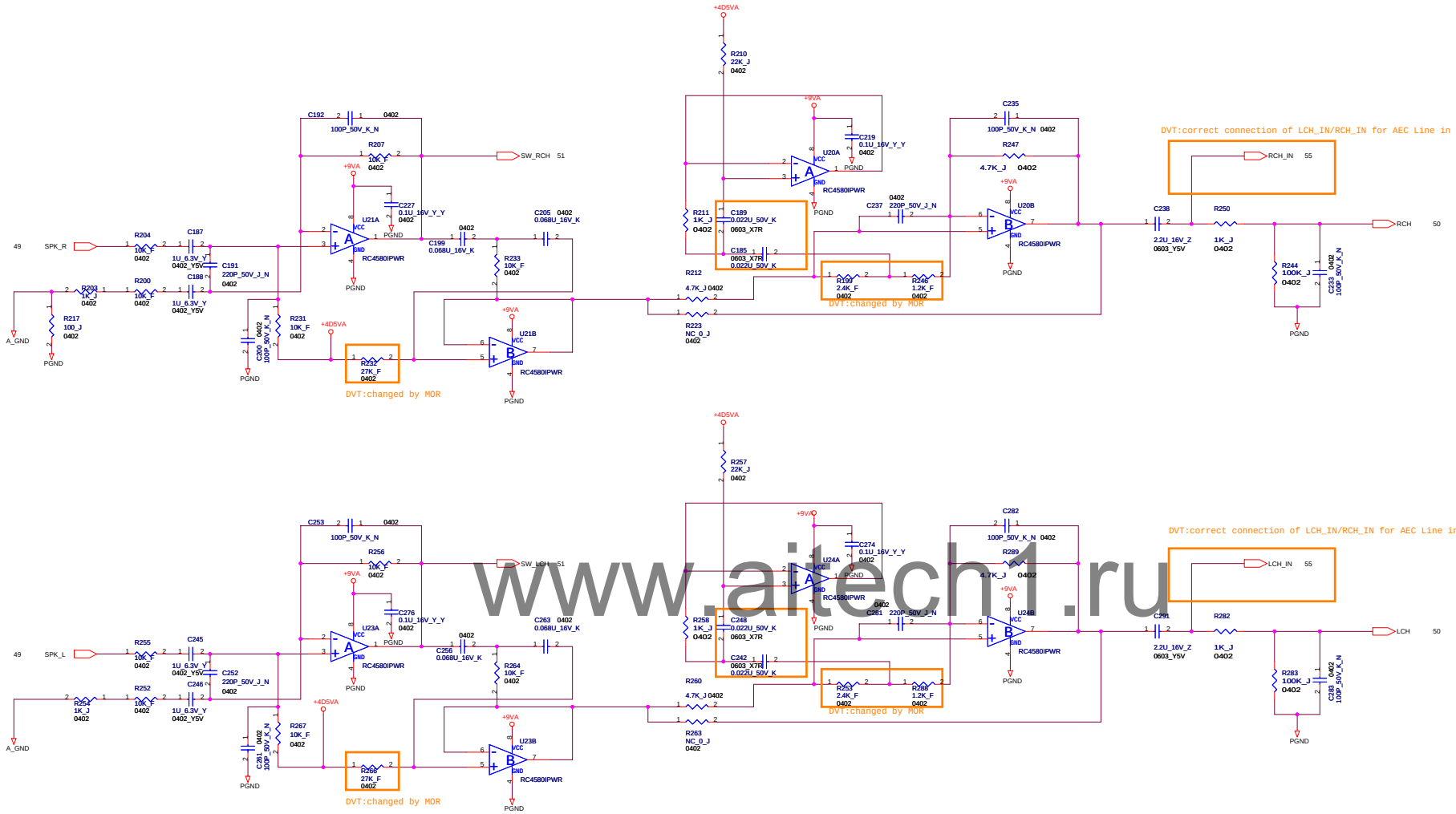


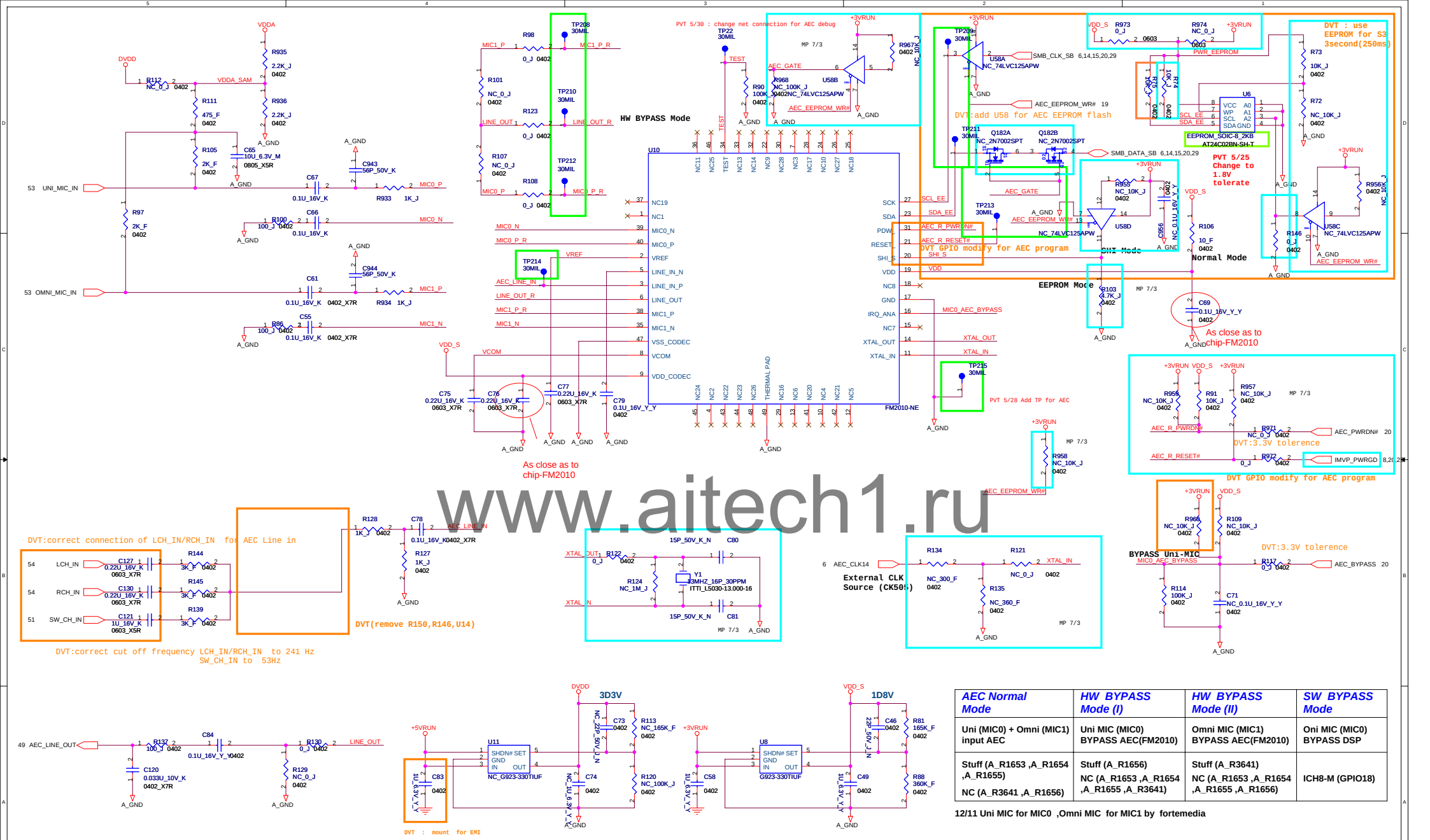


Array Microphone To AEC DVT change to 6pin

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO (MUTE & INT MIC)	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 53 of 71	



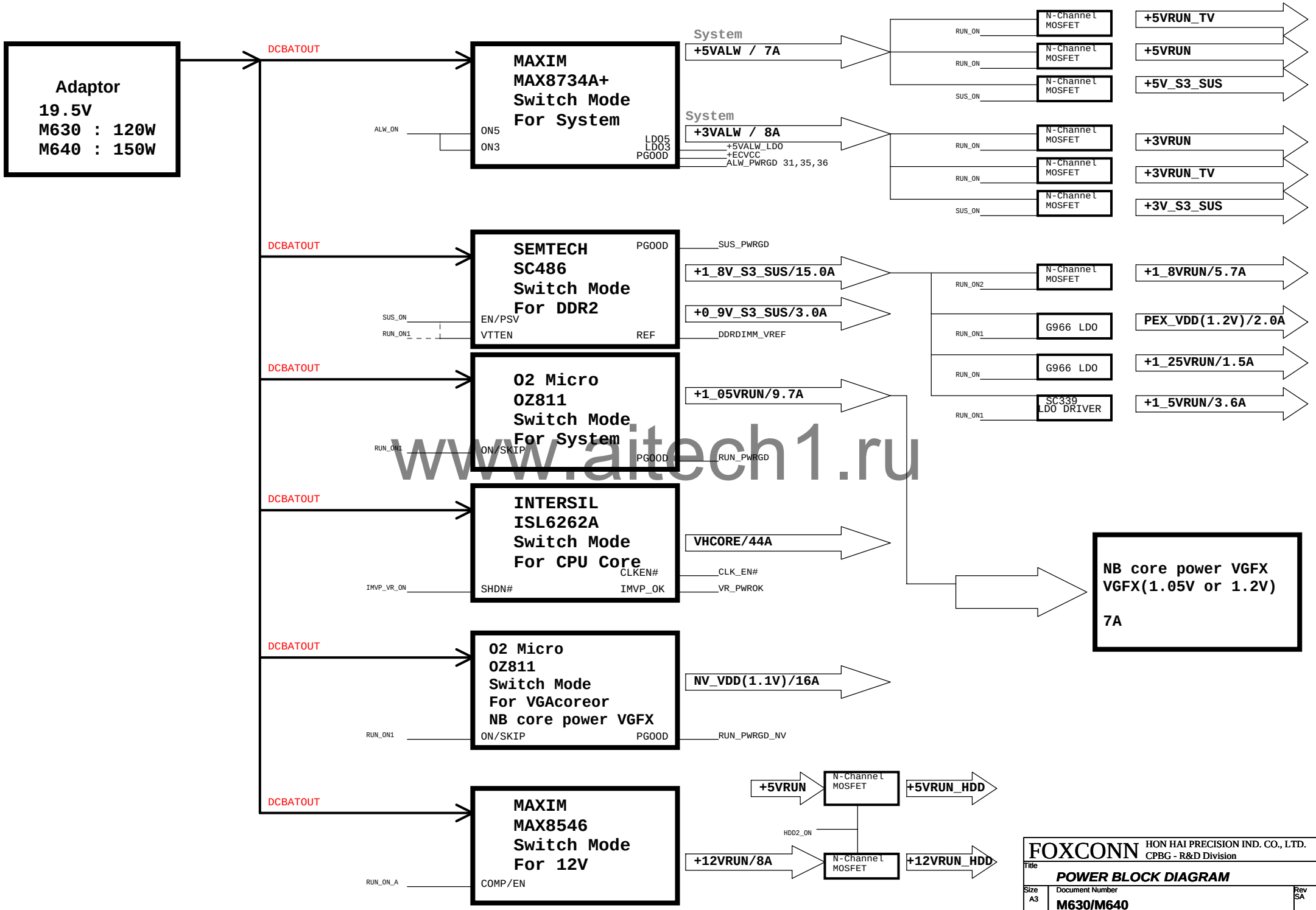
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	AUDIO(EQ)
Size A2	Document Number M630/M640
Rev	SA
Date: Wednesday, July 11, 2007	Sheet 54 of 71



AEC Normal Mode	HW BYPASS Mode (I)	HW BYPASS Mode (II)	SW BYPASS Mode
Uni (MIC0) + Omni (MIC1) input AEC	Uni MIC (MIC0) BYPASS AEC(FM2010)	Omni MIC (MIC1) BYPASS AEC(FM2010)	Oni MIC (MIC0) BYPASS DSP
Stuff (A_R1653 ,A_R1654 ,A_R1655) NC (A_R3641 ,A_R1656)	Stuff (A_R1656) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R3641)	Stuff (A_R3641) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R1656)	ICH8-M (GPIO18)

12/11 Uni MIC for MIC0 ,Omni MIC for MIC1 by fortemedia

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	AUDIO (AEC)
Size: Custom	Document Number: M630/M640
Rev	SA
Date:	Wednesday, July 25, 2007
Sheet	55 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
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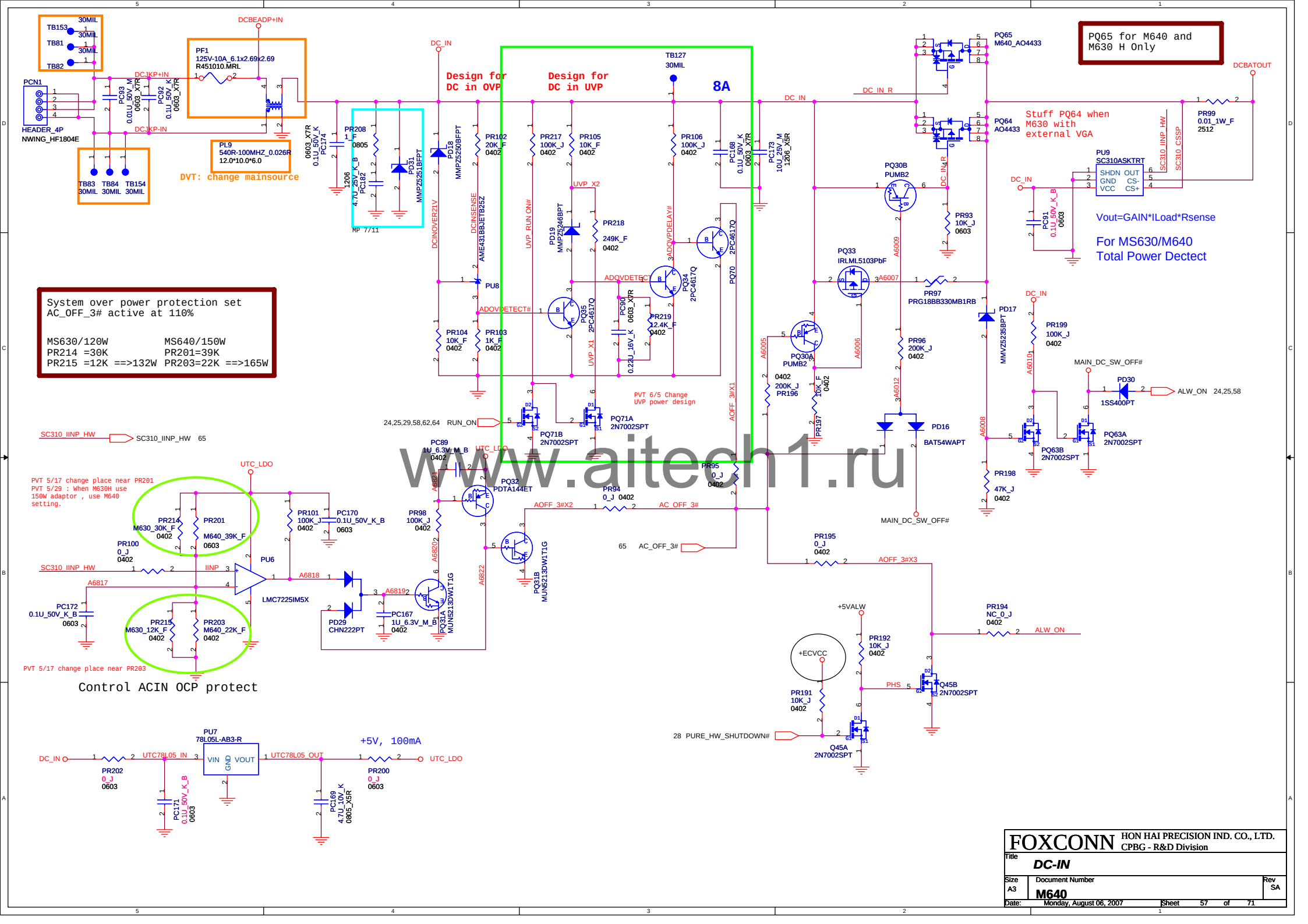
Title: POWER BLOCK DIAGRAM

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 56 of 71


PQ65 for M640 and M630 H Only
Design for DC in OVP
Design for DC in UVP
8A
Stuff PQ64 when M630 with external VGA
Vout=GAIN*ILoad*Rsense
For MS630/M640 Total Power Dectect
System over power protection set AC_OFF_3# active at 110%
MS630/120W PR214 =30K PR215 =12K ==>132W
MS640/150W PR201=39K PR203=22K ==>165W
PVT 5/17 change place near PR201
PVT 5/29 : When M630H use 150W adaptor , use M640 setting.
PVT 5/17 change place near PR203
Control ACIN OCP protect
PVT 6/5 Change UVP power design
DVT: change mainsource
+5V, 100mA
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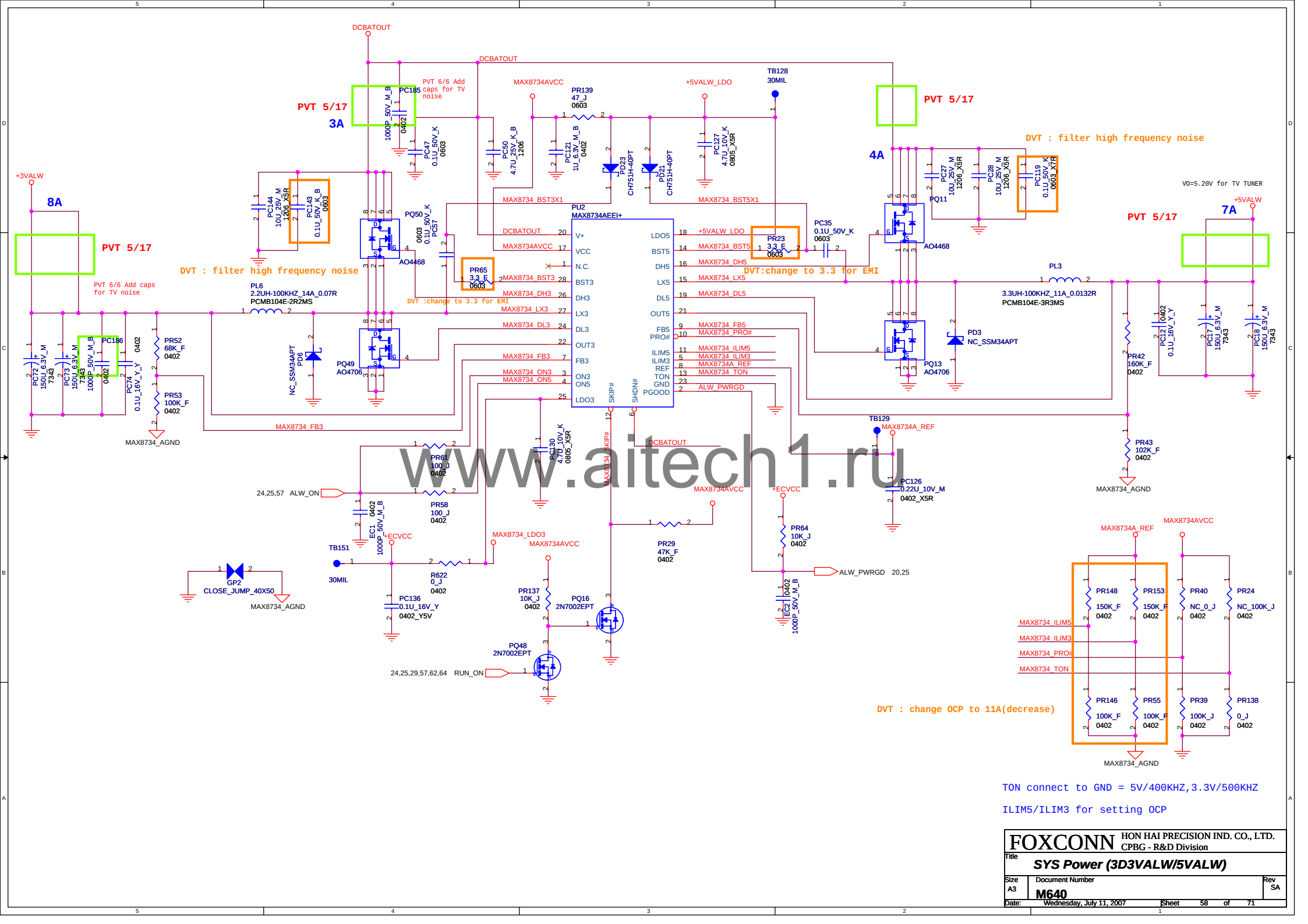
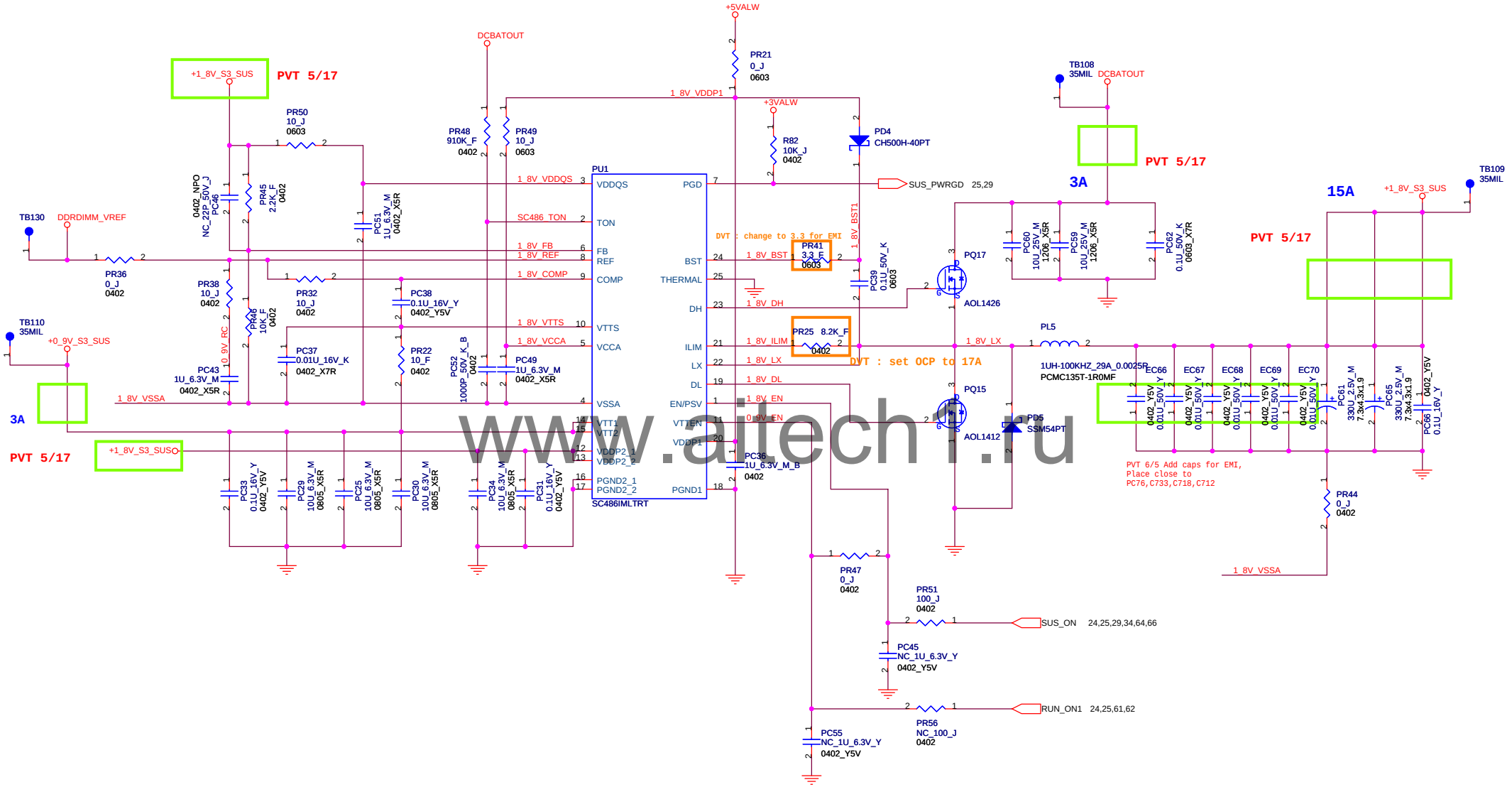
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
DC-IN
M640
Monday, August 06, 2007



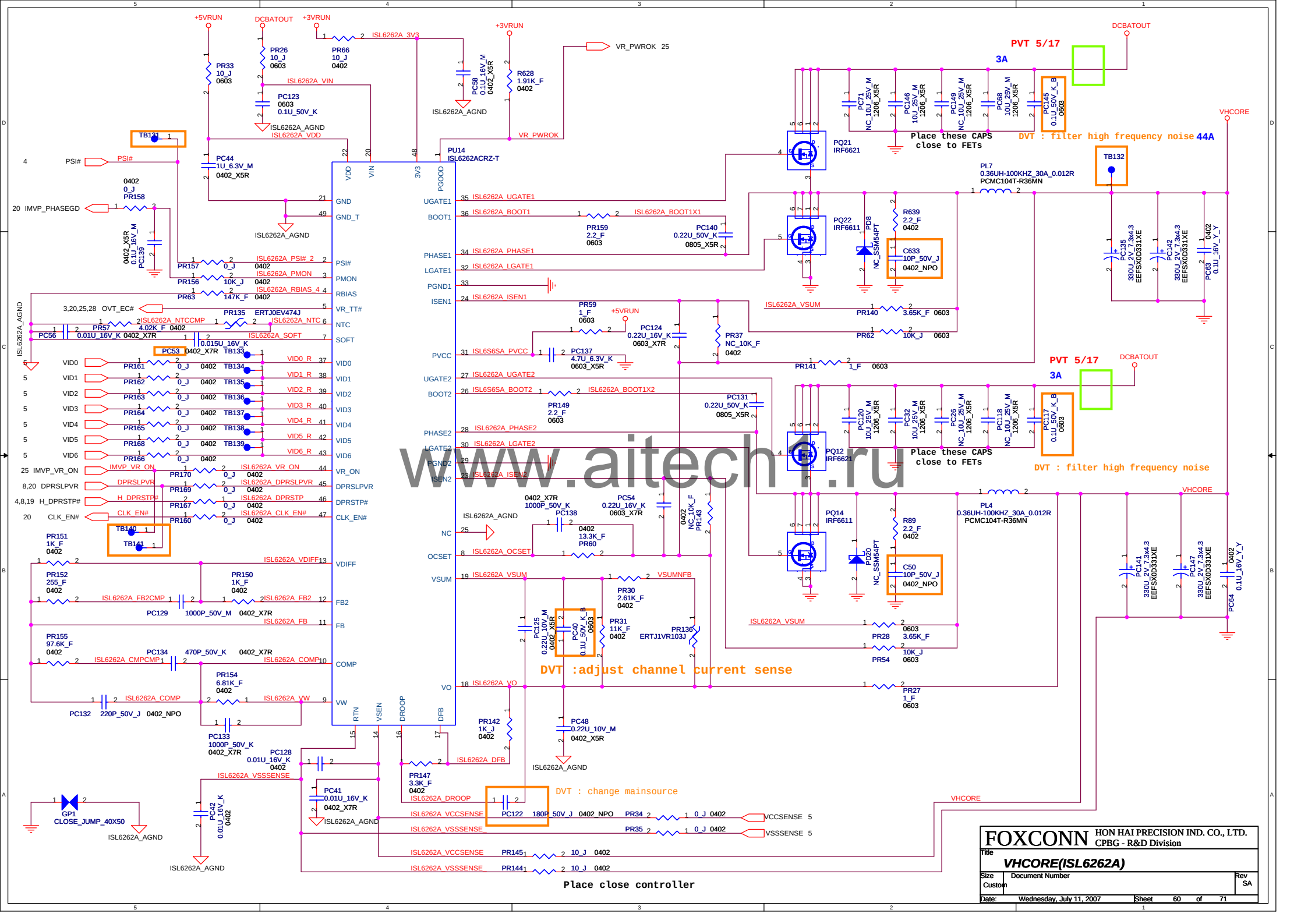


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

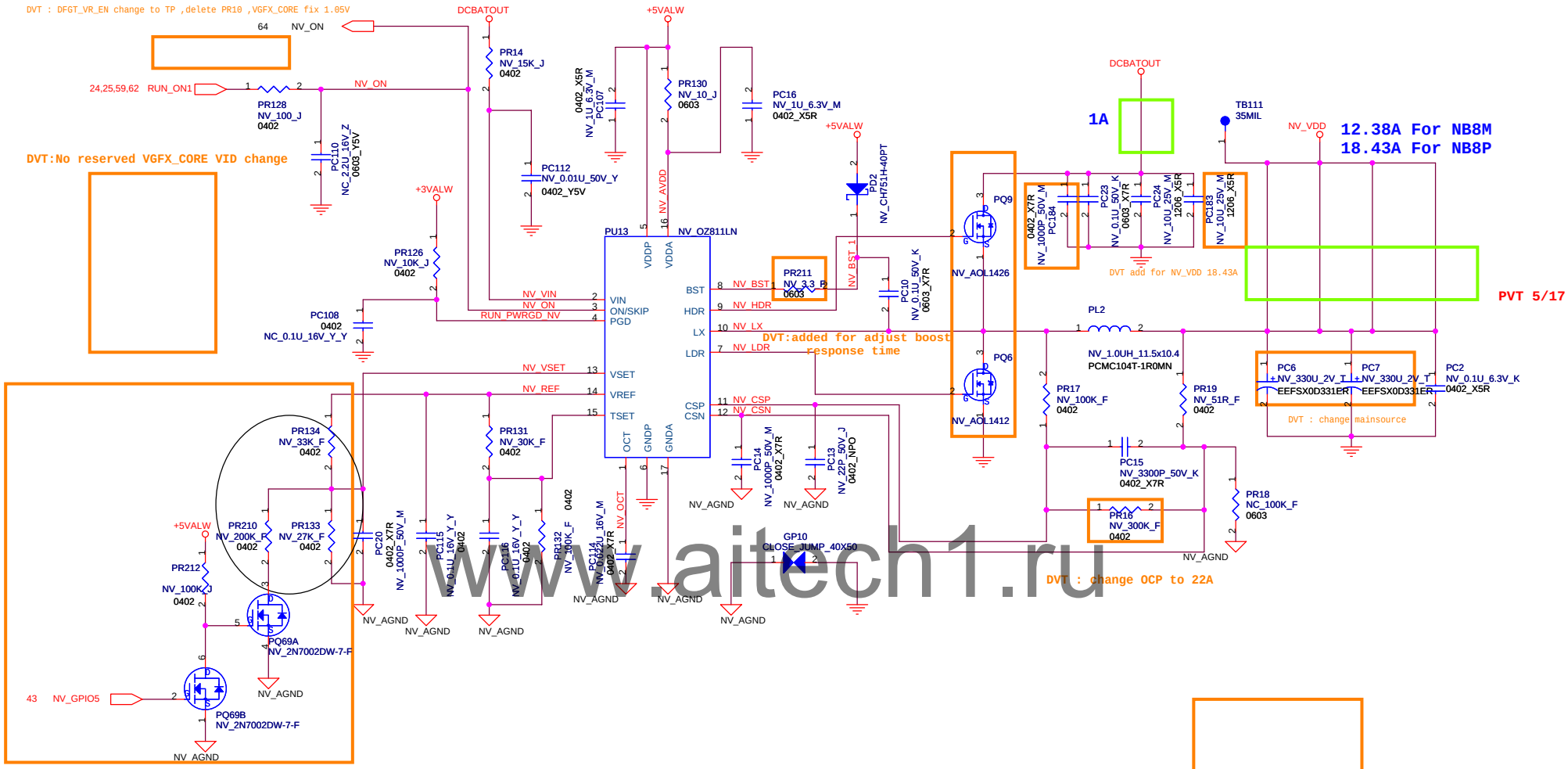
Title: DDR2Power(+1_8V_S3_SUS/+0_9VRUN)

Size: A3 | Document Number: M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 59 of 71



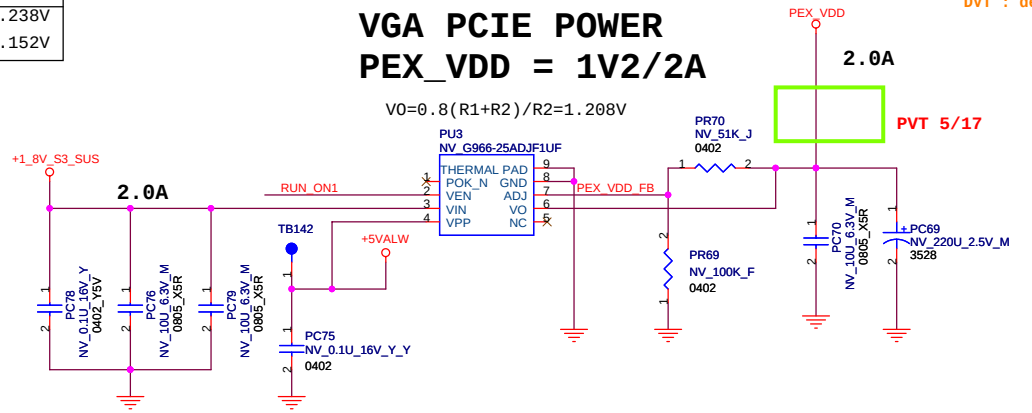
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VHCORE(ISL6262A)
Size	Custom
Document Number	
Rev	SA
Date:	Wednesday, July 11, 2007
Sheet	60 of 71



	I/O	Inter pull low	GPIO TABLE
GPIO5	O	Yes	GPU Voltage H: NVDD=1.238V GPU Voltage L: NVDD=1.152V

VGA PCIE POWER
PEX_VDD = 1V2/2A

VO=0.8(R1+R2)/R2=1.208V



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA POWER(GMCH)

Size: A3 | Document Number: M630/M640 | Rev: SA

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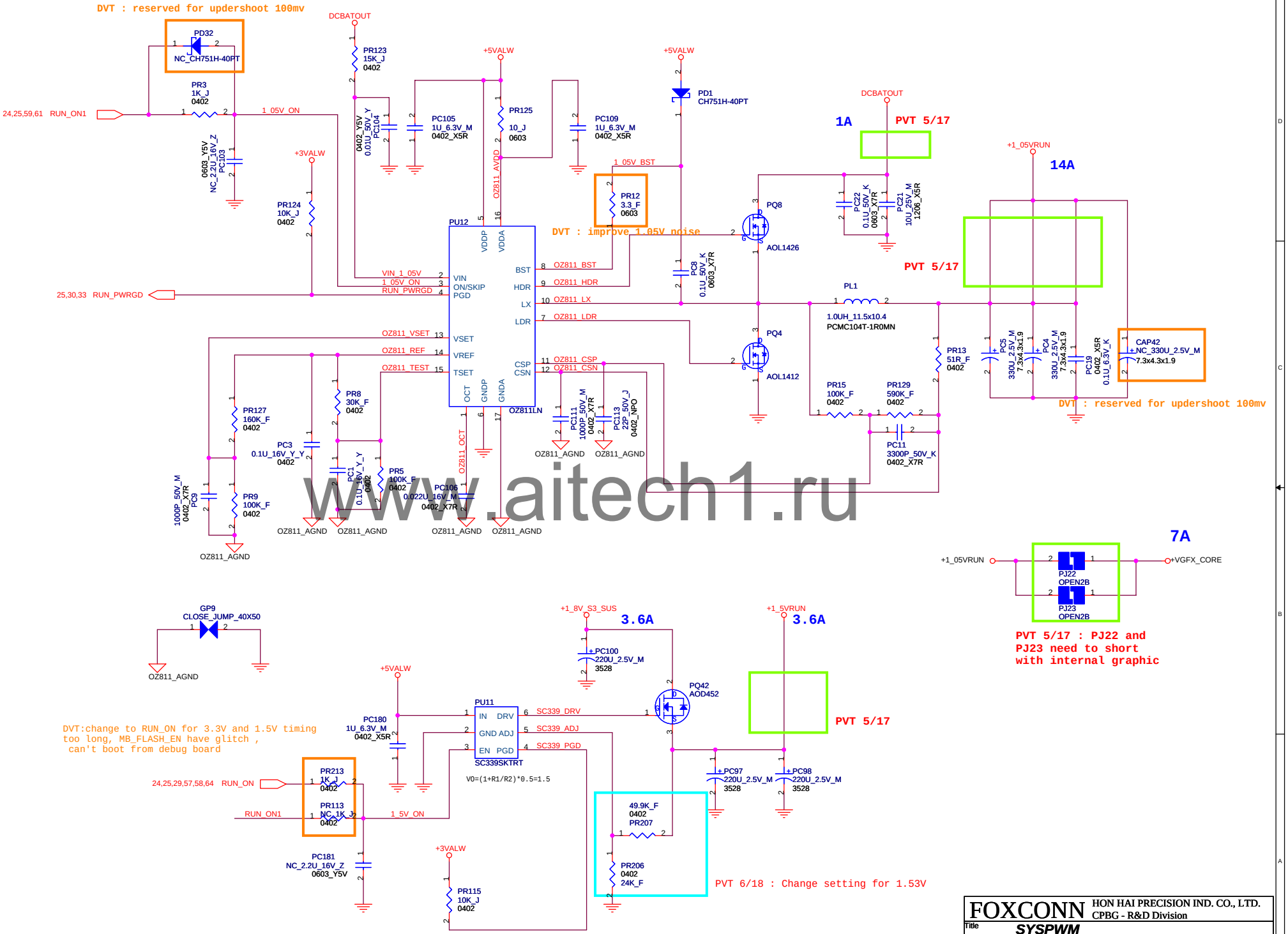

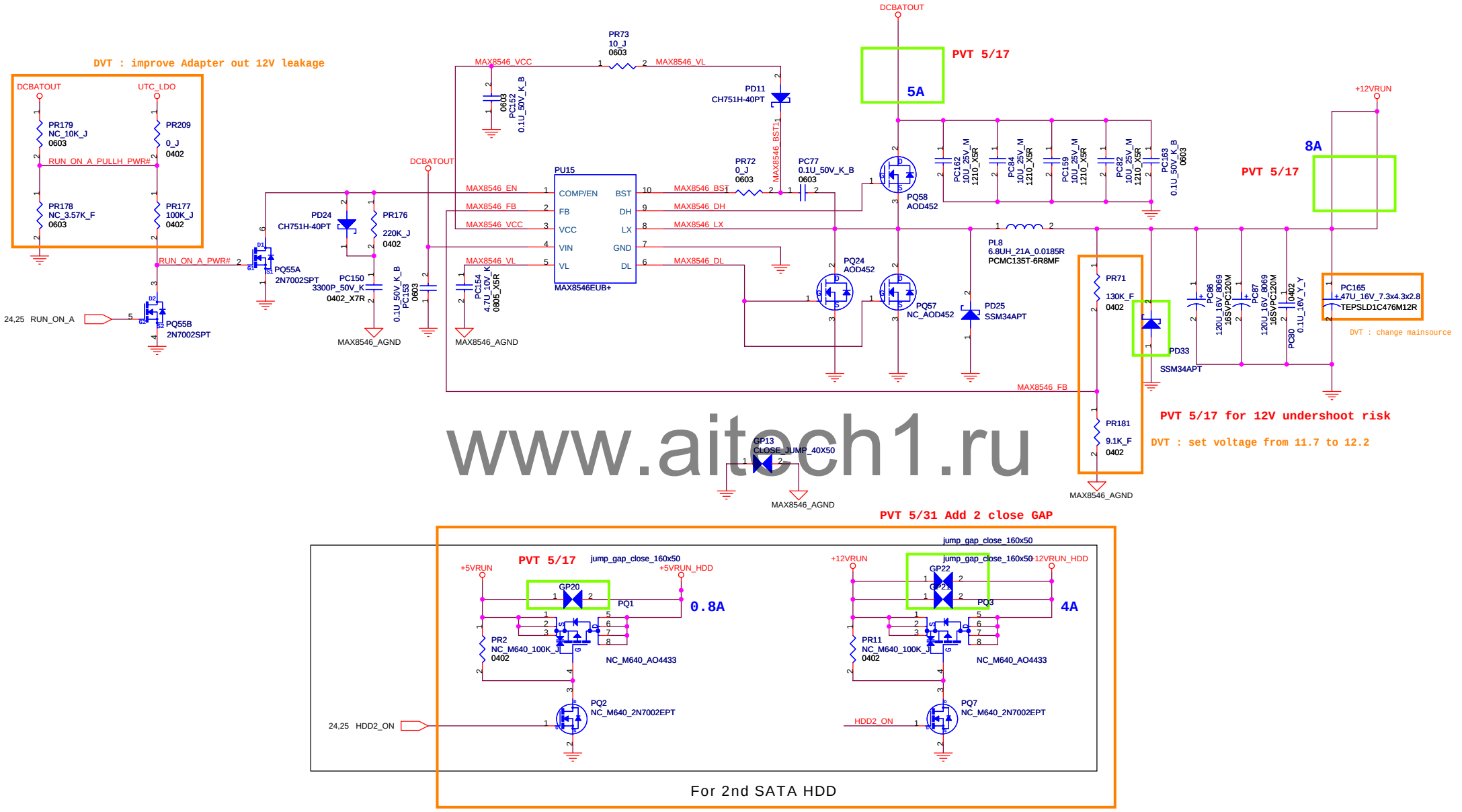

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: +12VRUN POWER(MAX8546)

Size	Document Number	Rev
A3	M630/M640	SB

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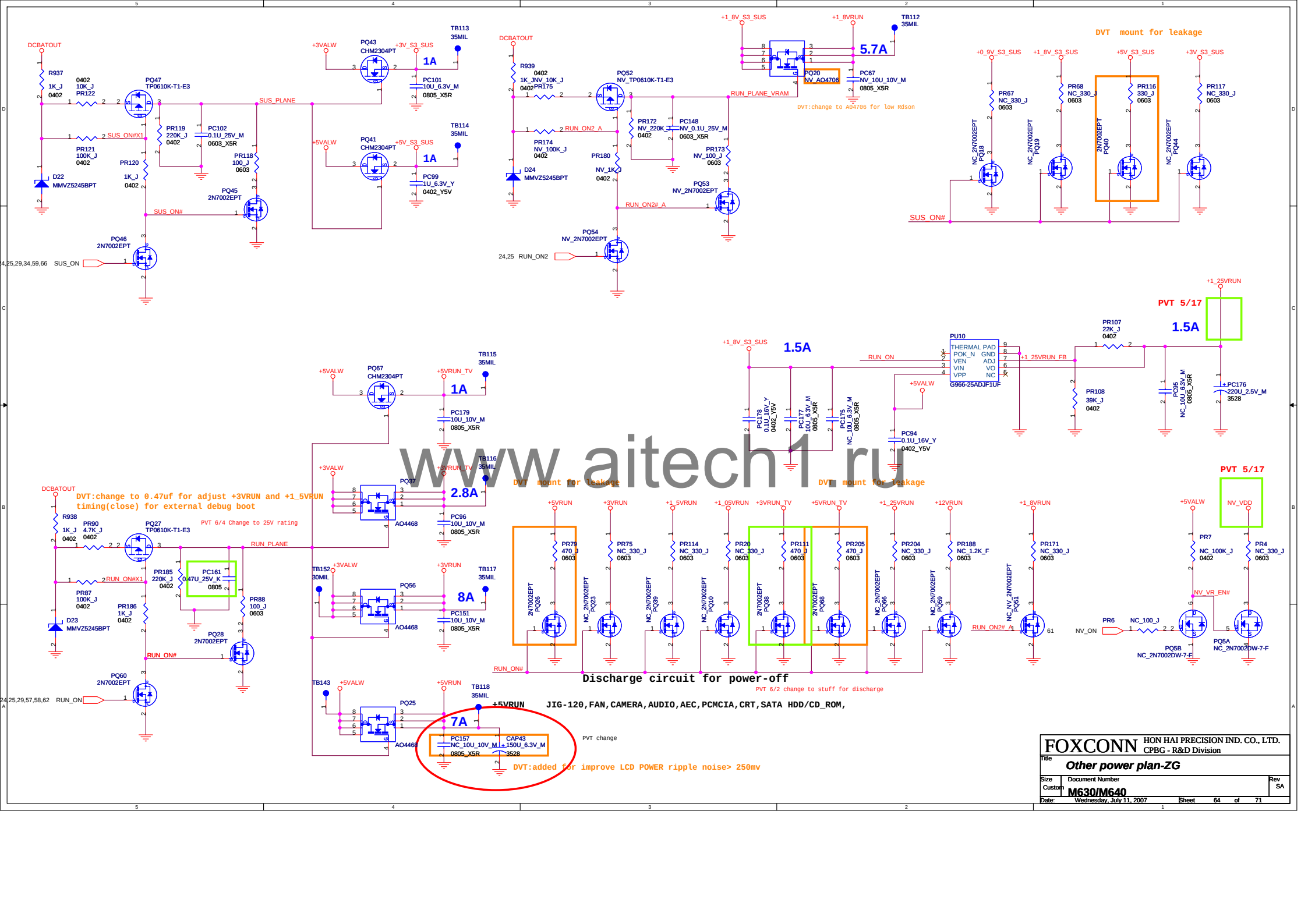

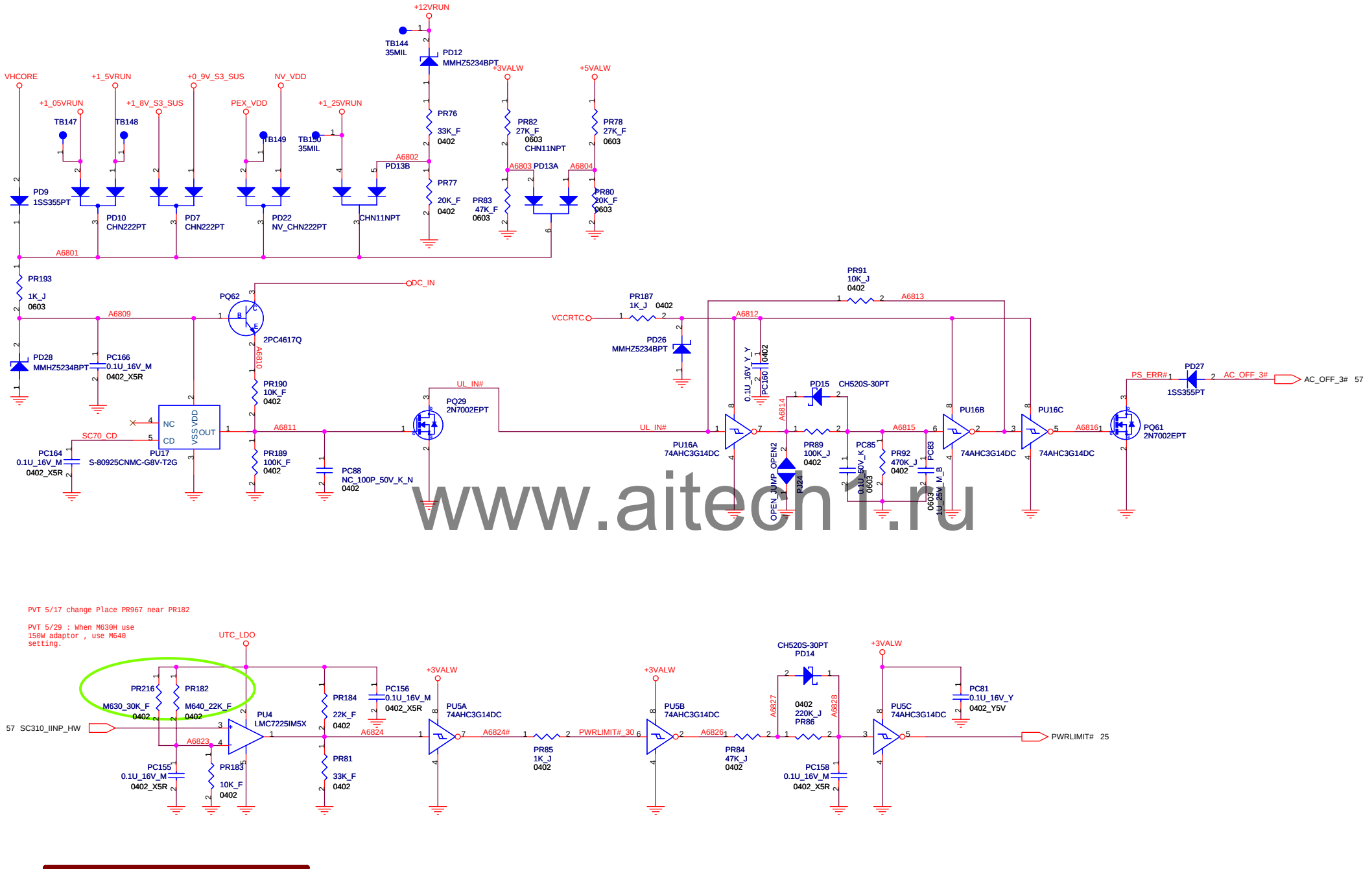

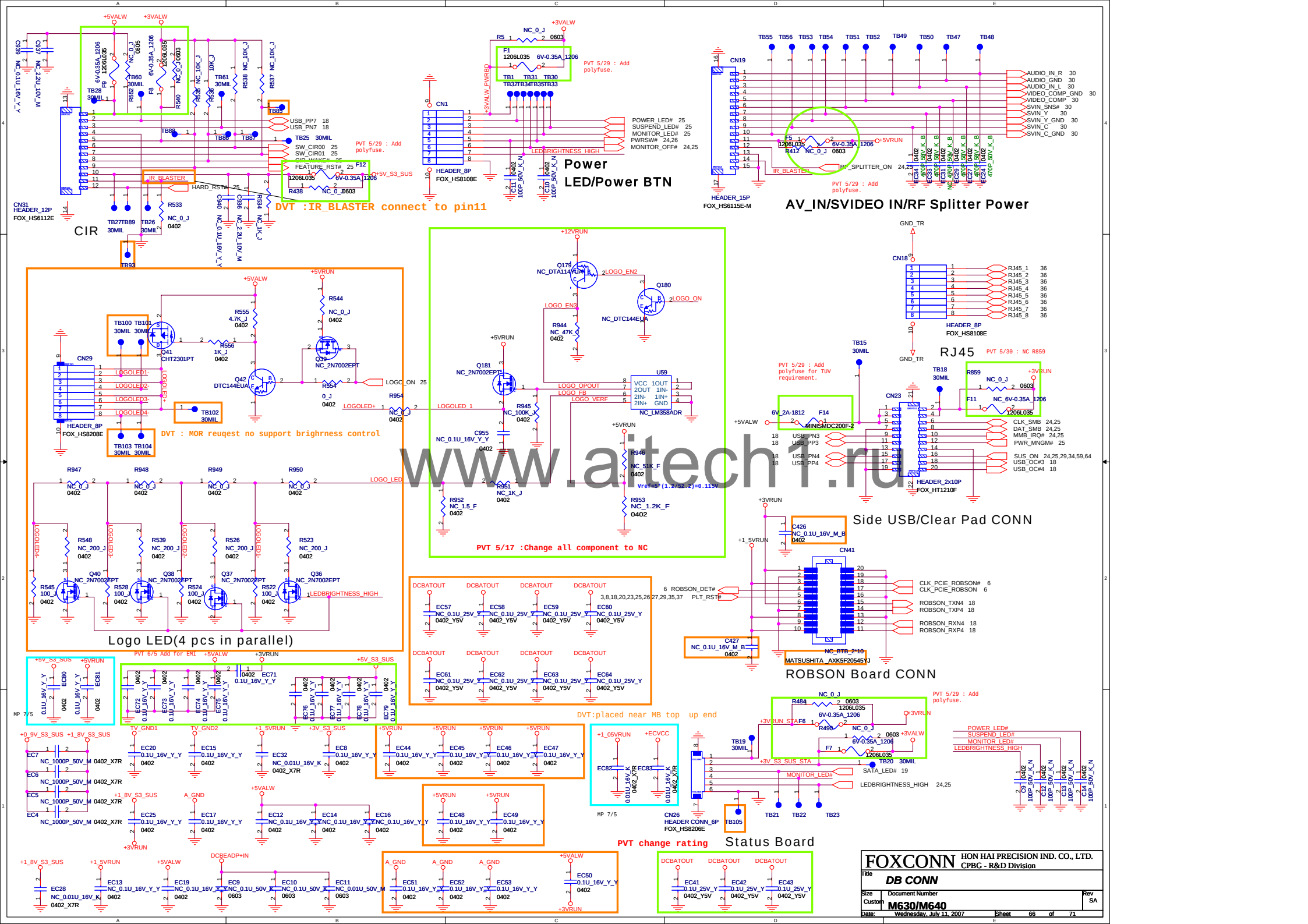

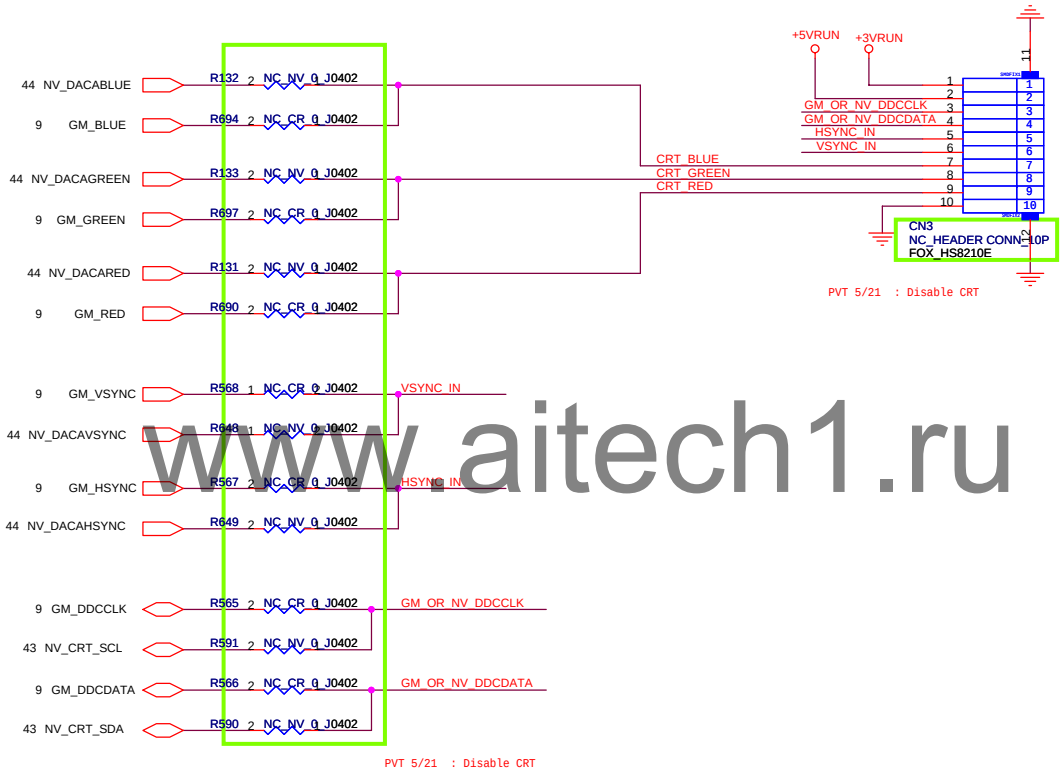

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M630/M640	Rev: SA
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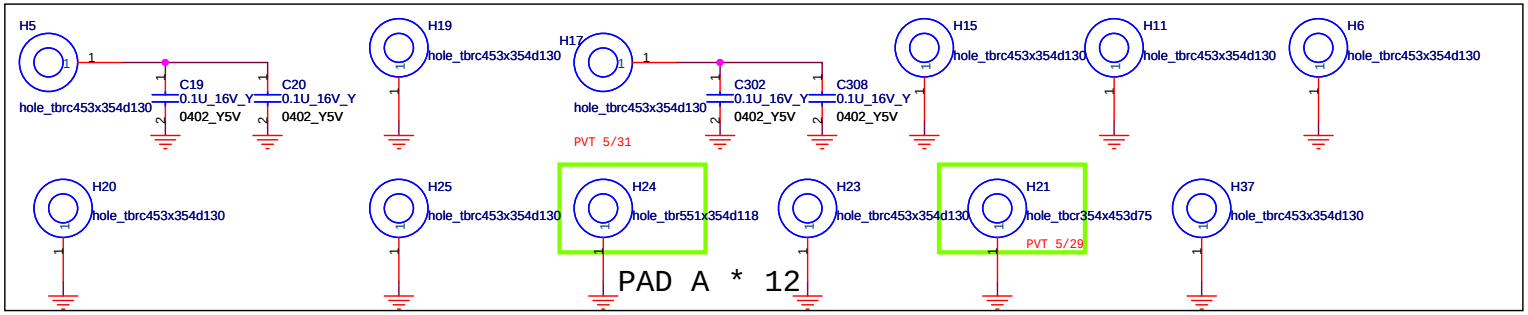

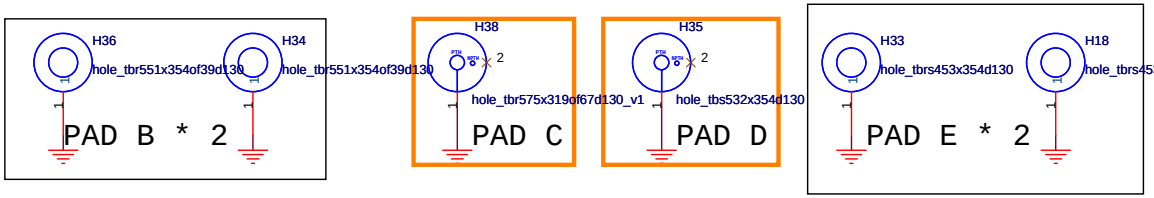

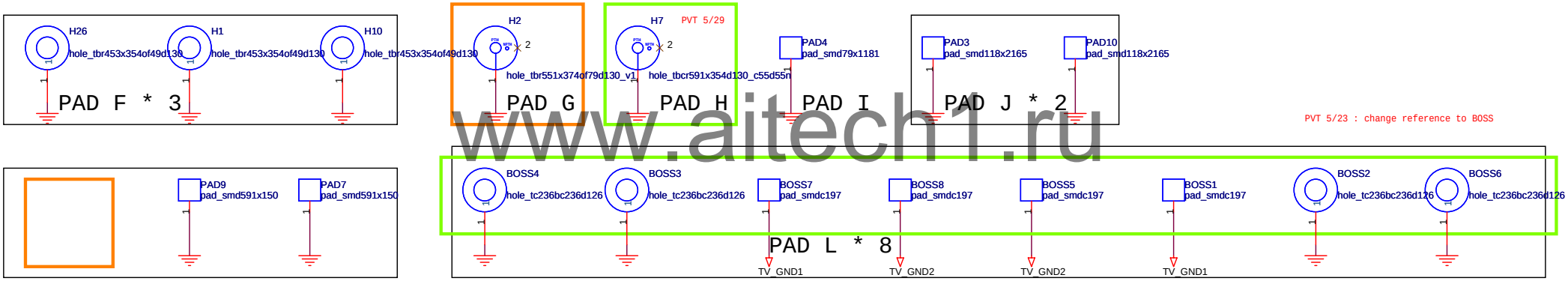

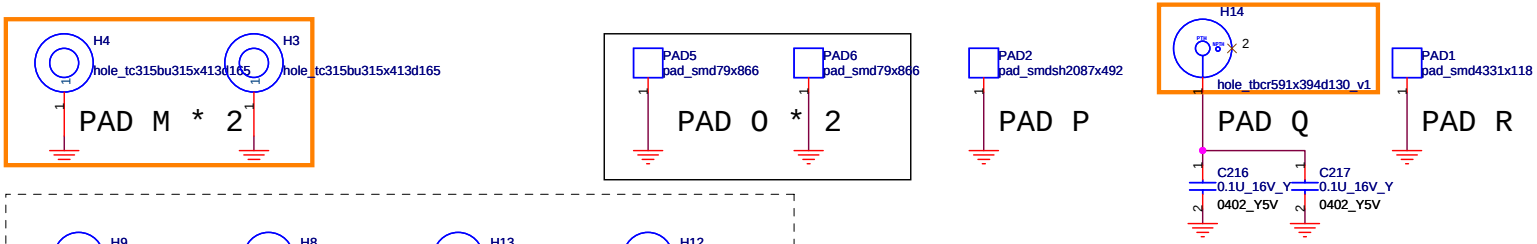

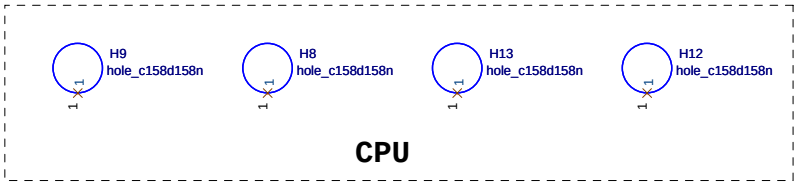

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **HOLE/BOSS PAD**

Size	Document Number	Rev
B	M630/M640	SA

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12/15
Change VRAM from " K4J55323QG-BC20" to "K4J52324QE-BC14 "

12/16
Add R3720
Update Library of CN30,CN31,CN26

12/18
Update screw hole/pad
Add R3721 NC_0 ohm
Change P/N of JSPK3 to HF5504 for current rating
Add R3722~3724 for EMI
NC RP1 (Default use Winbond EC)
Change U22/U23/U26 to G545 for safety certification
Add C3680~3685 for EMI
Remove R2007 resistor.
N.C. R2017
Delete R1994, L83, L84, L85, C1634, C1640, C1647.
Update symbol & footprint of CN41(SPDIF)
Update Ex-GFX Configuration on P.38

12/19
Back-annotation 08:24AM
Change R522,R523,R524,R526,R528,R539,R545,R548 to 200 ohm
Add Q178,R919,Q177,R920 for WoWLAN on S4 support.
Delete Q33, R438 for not supporting half brightness control of WLAN LED
Change R428 value to 68 ohm for brightness adjustment
N.C. R872, STUFF R873
N.C. R457, STUFF R453
N.C. R462, STUFF R461

12/20
Re-assign GPIO pin of EC
N.C. R535
Delete L33,R371,R436
Add R438,R928,R929,R930,R931
N.C. C325,C365
Add C936~940

12/21
1.@p23CAP1,CAP34 change to 47uF16V 1C-44T0476-M300
2.@p51CAP16,CAP17,CAP18,CAP19,CAP20 change to 47uF16V 1C-44T0476-M300
3.@p63PC165 change to 47uF16V 1C-44T0476-M300
4.@p59PQ17 change to AOL1426 17-A0L1426-0000
5.@p59PQ15 change to AOL1412 17-A0L1412-0000
6.@p62PQ8 change to AOL1426 17-A0L1426-0000
7.@p59PQ4 change to AOL1412 17-A0L1412-0000
8.@p57PQ64,PQ65 change to AO4433
9.@P63PQ1,PQ3 change to AO4433
10.@p58PQ11,PQ50 change to AO4468 17-A0L4468-0000
11.@p61PQ9change to AO4468 17-A0L4468-0000
12.@p64PQ20,PQ25,PQ37,PQ56 change to AO4468 17-A0L4468-0000

12/21
Delete R492,R876
Delete net "VDDA_M". Add R935,R936
Change PURE_HW_SHUTDOWN# pull high power from +5VALW to +ECVCC(PR191)
Add PR208,PC182,PD31
Add R492 for LEDBRIGHTNESS_HIGH pull down
Change Q178 to PMV65XP for lower Rds(on) and voltage ripple

12/22
N.C. R815,EC31
Add Net "USB_VCC0_R", "USB_VCC1_R","USB_VCC2_R" for USB connector
Change CAP16~20 value to 68uF
Change PJ33 to larger pad open jump
Add PJ35 for higher current requirement for NB8P

12/23
Change H16 net to TV_GND2, H30 to TV_GND1
Add R937,R938,R939,D22,D23,D24 to prevent 2N7002 from damage if DC_IN is over 20V
N.C. KB3910SFC1 to create BOM for factory (Winbond will be used in EVT by default)

12/25
P.41,P.42,P56,P.61 Change description of current (Ampere) requriement for NV_VDD & FBVDDQ
Connect H21, H37 to GND
Delet EC23,EC8,EC22,EC30,EC26,EC21
Add C946~949 for vista requirement
Change VGA Straping resistors to set NB8M-GT, Qimonda 256MB as default
Add net THERMTRIP_GFX#_R to KB3910S

12/26
N.C. R521,R543
Mount R274,R275

12/27
N.C. All Winbond EC parts
N.C. RP38
Update SYSTEM_ID Table

12/28
N.C. C749
Add prefix NV_ FOR R572
Delete prefix NV_ for C503
Change value to from 39 to 33ohm(R861/R857/R488/R485/R480/R481/R864/R863)
Change R467 value from 33K to 0 Ohm
Change C433/C434 value from 6.8pf to 10pf
N.C. R466,R305

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070206
P06 update U49 symbol data to ICS9LPR358AGLFT
P55 remove R150,R146,U14 short R128 pin1 and R145 pin2 for AEC function fail

0301
NV design change
change R596 from 30 to 24.9ohm
change R502 from 40.2 to 45.3 ohm
change R52,R93,R17,R561 from 240 to 0 ohm
R56,R95,R19,R560 from 240 to 243 ohm
change R1,R10,R18,R32,R36,R80,R102,R563 from 7.5k to 4.02k ohm

0302
P53 modify netname for netname consistance for UNI_MIC_IN and OMNI_MIC_IN
P25 add R940,R941 for KBC strap pin pull low
P30 add C950 for RUN_PWRGD interferenced ,hang 49
P24 mount R398 for THERMTRIP_GFX#_R disconnection
Crystal vendor suggestion
(1)P19 change C874,C873 to 12P
(2)P24 change C433,C434 to 12P
AEC EEPROM mounted for S3
P55 mount R72,U6,R75,
NC R92,R96,R104
AEC programming GPI change
P20 GPIO24 connect to AEC_PWRDN# for power down AEC
GPIO20 connect to AEC_RESEt# for programming AEC
Brightness control not support for Logo LED
P66 (1)NC Q36,R523,Q37,R526,Q38,R539,Q40,R548
(2)change R545,R58,R524,R522 from 200 to 100 ohm
Mount parts for leakage
P64 mount PR116,PQ40,PR205,PQ68,PR79,PQ26
MB_FLASH function fail :change MB_FLASH_EN from SB GPIO 26 to GPIO34,GPIO26 can't used as GPIO
P20 connect GPIo6 to TP206 , connect GPIo34 to MB_FLASH_EN ,add R942
change 2nd and 3rd fan from 12V to 5V , change Q52,Q13 to CHT2301 for 5V source

P51 NC R342 for subwoofer abnormal performance
P24 add C951 for thermistor interference by inverter transformer
P50 change F3 to 1M-F1252A5-F000 for the same with M620
P51 change F10 to 1M-F1252A5-F000 for the same with M620

0305
P20 change R844 to 10K, LAN_RST# change to pull low 10K

0306
POWER
P58 change PR148,PR153 to 150K_F,PR146,PR55 to 100K_F
to change ocp setting to 11A
P61 (1)change PR16 to 1M_F to change OCP to 15A
(2)delete PJ10,PJ9 ,VGFX_CORE from NV_OUT
P63 change PR71 to 130K_F,PR181 to 9.1K_F , change 12V from 11.7 to 12.2v
P59 change PR25 to 8.2K_F to set OCP to 17A
P60 mount PC145,PC117 to filter high frequency noise
P58 mount PC119,PC143 to filter high frequency noise
P62 change PR12 to 3.3_F to improve 1.05V noise
P63 change PR177 to 100K_J,add PR209,NC PR179,PR178 for improve
adapter out 12V leakage

P33 modify CN36 symbol for PCMCIA reverse type,
P35 change ln power to +3V_EMINI_AUX to support S4 wake up

0307
P50 change U26,U27 to LLP package for support 3W
P61 change PQ9 to AOL1426 ,PQ6 to AOL1412 for support 15A NV_VDD
P34 change U41,U40,U39 to MSOP8 to meet EUV 2.4mm

0309
correct EVT BOM mian source to Substitute List
(1)P50,P60 change PC53,C913,C924 to 1C-2B20153-K000
(2)change C468,C475,C480,C907 to 1C-2B20471-K000
(3)P11,P12,P50 change C265,C284,C286,C722,C710,C738,C303 to 1C-2B20474-K000
(4)P50,P51 change L24 ,L59 to 1L-BBCMS32-1600
(5)P57 ,change PL9 to 1L-FBHWP12-1000
(6)P49 ,change C241,C243,C247,C250 to 820P NPO 0603
(7)P60 ,change PC122 to 1C-2N20181-J600
P25 delete Winbond solution

0313
P60 change PC40 to 0.1u to adjust channel current sense by vendor suggestion
P54 change U16 to 78L09L , the same with M620
P61 add PR210,PQ69,change PR133 to 28K_F for VGA power mizer(1.2V and 1.15V switch)
P43 connect NV_GPIO5 to VGA power for power mizer(1.2V and 1.15V switch)
P43 change R930,R931,C938 value to NV_*
P06 connect R752 pin 1 to R750 pin1 to follow CPU_BSEL0
P27 change LED1 to HT-110NG for changing wlan led to side
P51 change CAP16~20 to 47UF for 6BUF shortage(evt used 47uf)
P50 change L67,L70 to EBMS100505H121RDC35 for changing mainsource(EVT use this part)

0314
P53 change CN7 to HS8106,防呆
P67 NC CN3(CRT CONN) for ME interfere with thermal module
P34 change CN24 to FOX_UB4132C-T3201-4F,black color
P31 change CN15 to FOX_UV91413-WS01P-4F,black color
P11 delete L12,C194,C211,L17,L16,C204,L14,C226,R230
Reserved R234 to +3VRUN and R236 to GND for UMA/Discrete selection,
Refer to Santa Rosa design Guide Rev 2.0 Table 81.

0319
Modify for Clock SI
P30 mount R790,0 ohm and C848,22P for PCI_CB48 SI fail]
P06,P27 change RP30 to 18 ohm ,add C 2.2p for CLK_PCIE_MINI# SI fail
P06 change RP24 to 15ohm for CLK_PCIE_SATA# SI fail

P29 swap L51,L50,L49 for layout

0322
MOR
P49 remove R279 for delete Line in path
P50 change C458,C478 to 1000P ,X7R for THD/MR improvement
P50 add C for U44 bypass
P50 change C924 and C913 to NC for THD/MR improvement
P50 change the connection of CON3 pin7 and pin8 to DGND
P50 change GP3 to 0ohm resistor (mounted)
P52 delete R774 and R767 completely for delete MIC VREF path from CODEC
P49 U22 pin32 change to NC for delete MIC VREF path from CODEC

P45 change C27,C33,C48,C57 to 0.01uf by nvidia FAE suggestion
P46 change C28,C947,C5,C21 to 0.01uf by nvidia FAE suggestion

EMI
P59 change PR41 to 3.3ohm for EMI
P58 change PR23,PR65 to 3.3 ohm for EMI
P19 add EC36,EC39,EC40 33P bypass for BITCLK

P55 mount C93 for EMI

0326
(1)add AEC_EEPROM_WR# for programming AEC EEPROM
(2)connect DFGT_VR_EN to TP and delete PR10 , VGFX_CORE 1.05V fix

0327
(3)reserved Linear voltage control circuit for logo led suddenly off (U59,Q180,Q179,Q18
(4)1.5V enable pin change to RUN_ON for no boot from ext debug board issue
add CAP41(470uF) for subwoofer +12V power

0328
(1)change C127 and C130 to 0.22uF, C121 to 1uF.
(2)change the connection of C127 to C291, C130 to C238, C121 to C324.
(3)change PR109 to 18K
(4)change R232/R266 to 33K
(5)change R199/R253 to 1.8K

0329
(1)change R424,R807 to 1K_J for follow M610(MOR request)
(2)remove NVIDIA NC pin TP to enlarge NV_VDD power plan
(3)add R962,R961,L71,L72,EC54,EC55,EC56 for EMI

0331
Reserved CAP42 and PD32 for 1.05V undershoot 100mV
Reserved R963 for S3 resume shutdown

0402
(1)change PC161 to 0.47uf ,50V for adjust +3VRUN and +1_5VRUN timing(close) for external debug boot
(2)reserved R964 for disable Thrmtrip

0403
add CAP44 for LVDS power ripple (too large,spec is 200mv)

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070602
Page 55 U6 change to 13-AT24C02-8001, add TP for AEC test usage.
Page 58 Remove PJ20,PJ21,PJ32,PJ31,PJ8,PJ11 .
Page 59 Remove PJ14,PJ15,PJ17,PJ18,PJ19 .
Page 60 Remove PJ16,PJ13.
Page 61 Remove PJ33,PJ12,PJ2,PJ6,PJ30,PJ35.
Page 62 Remove PJ7,PJ3,PJ4,PJ5,PJ28.
Page 63 Remove PJ26,PJ27,PJ25, Change PR1 and PJ1 to close gap GP20, GP21,GP22
         Add PD33 at +12VRUN output.
Page 64 Remove PJ34.
Page 33 CAP3 change to 1C-44R0476-M200.
Page 27 LED1 change to HT-110UYG.
Page 24 NC SW3 and change to resistor for System ID control
Page 50 change R966 to stuff and R965 to NC.
Page 9   Change to NC : R675, R667, R225 Change to Stuff : R221, R214, R693,
         R696, R689, R691, R692, R688, R687 for disable CRT function.
Page 11 Change from stuff to NC :L44,L45,C731,R224,C197,L13,R679,R234,R685,L47,C735,L48,
         Change from NC to stuff : R683,R227,R677,R236,R686,R699 for disable CRT function.
Page 66 Change from stuff to NC :Q179,Q180,U59,R946,R953,R951,R952,C955,R945,Q181,R944
         to remove 2nd logo LED solution.
Page 57 Add PR214 to 30K ohm, PR215 to 12K ohm, Change PR203 to 22K ohm, PR201 to 39K ohm.
         To set the different setting for M630 and M640.
Page 65 Add PR216 30K ohm, change PR182 22K ohm, change PR183 10k ohm.
         To set the different setting for M630 and M640.
Page 49 Change CN21 to 2N-0006000-FET0.
Page 17 Add ESD diode D25 for INV_ENABLE and INV_BRADJ signal for U17, U35 damaged issue.
Page 3   Remove TP :TP140,TP146,TP127,TP134,TP125,TP137,TP126,TP157,TP133,TP148,TP142,TP136
         ,TP120,TP141,TP128,TP119,TP135,TP156
         to Remove test point for interference with CPU bracket.
Page 20 NC SW4 and use resistor for system ID control
Page 4   Remove TP159,TP124, TP158,TP32 for not interference with CPU bracket.
Page 40 NC :L5,C70,C595,C608, Change to pull down 10K ohm : R115,R614,R621 diable CRT function.
Page 67 NC : R132,R694,R133,R697,R131,R690,R568,R648,R567,R649,R565,R591,R566,R590,CN3
         Disable CRT function.
Page 50 Change F3 to 4A capability.
Page 34 Change C469,C449,C430 to 1C-2B30105-M000 : 25V rating component
Page 44 Change to NC : R647,R645,R646,R626,R609,R610,R611,R634,R635,R624 Disable CRT
Page 52 Change C138,C167 to 4.7u_16V_0805(1C-2B70475-K300) for audio precision test result.
Page 52,50 change CON1, CON2 , CON3 vendor part number.
Page 68 Change nut pad reference to BOSS for factory requirement.
Page 46,45 Remove R52, C39, R17, C24, R561, C487, R93, C63 change Vram clock termination.
Page 25 Reserve caps C957,C958,C959 for Fan_tach signal noise improvement.
Page 57 Add PD34 for different setting for M640.
Page 55 Change net connection for AEC debugging.
Page 28 Change R138 to 8.2K and C82 to X7R for T8 setting to 110 celcius degree.
Page 66, 34 Add F13 and F14 for TUV spec.
Page 52 Change R786 and R782 to 6.8K Change resistor value to meet FSIV 2.0.
Page 66 Change to polyfuse 1M-F006A35-F000 0.35A rating from using 0 ohm at DVT.
        (F1,F4,F5,F6,F7) F2 use 0.5A rating.
0604
Page 14,15 Change C125, C122 to X5R rating for high temperature near Dimm module.
Page 20 Add C960 0.1uF at IC power pin.
Page 17 change C389 from 1uF to 0.1uF.
Page 64 Stuff PR111 and PQ38 for +3VRUN_TV discharge slow.
0607
Page 57 Implement new UVP protect circuit to prevent insert different adaptor risk.
Page 59 Add EC66,EC67,EC68,EC69,EC70 to +1_8V_S3_SUS to GND for EMI solution.
Page 66, 52 Add EC72,EC73,EC74,EC75 +5VALW to GND ,EC71 +5VALW to +5VALW , EC76, EC77, EC78
         , EC79 +5V_S3_SUS to GND for EMI solution. Page 52 EC65 A_GND to GND, Place near L71.

Page 45,46 Reserver 8 caps for Vram power and place 2 pcs for each Vram.
Page 58 Add PC186, PC185 at +3VALW input and output for noise improvement.
Page 25 Add R969 for +ECVCC discharge path reservation.
Page 57 Add PR219 for the discharge of UVP protect circuit, and change PR105 to 10K,
         PR218 change to 249K for tolerance control.
Page 34 Change from 0 ohm to common choke for EMI request on all USB port.
Page 28 Change Fan3 circuit for stuff at M630 only.

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